

ESM-CDV

COM Express Type 2 CPU Module

Quick Installation Guide

1st Ed – 16 November 2012

Notice

This guide is designed for experienced users to perform quick setup of the system. For detailed information, please always refer to the electronic user's manual.

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Part No. E2017286400R

FCC Statement



THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRE OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

THESE LIMITS ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST HARMFUL INTERFERENCE WHEN THE EQUIPMENT IS OPERATED IN A COMMERCIAL ENVIRONMENT. THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE HARMFUL INTERFERENCE TO RADIO COMMUNICATIONS.

OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE HARMFUL INTERFERENCE IN WHICH CASE THE USER WILL BE REQUIRED TO CORRECT THE INTERFERENCE AT HIS OWN EXPENSE.

Notice

This guide is designed for experienced users to setup the system within the shortest time. For detailed information, please always refer to the electronic user's manual.

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Quick Installation Guide

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To receive the latest version of the user's manual; please visit our Web site at:

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1. Getting Started

1.1 Safety Precautions

Warning!



Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!



Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

1.2 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

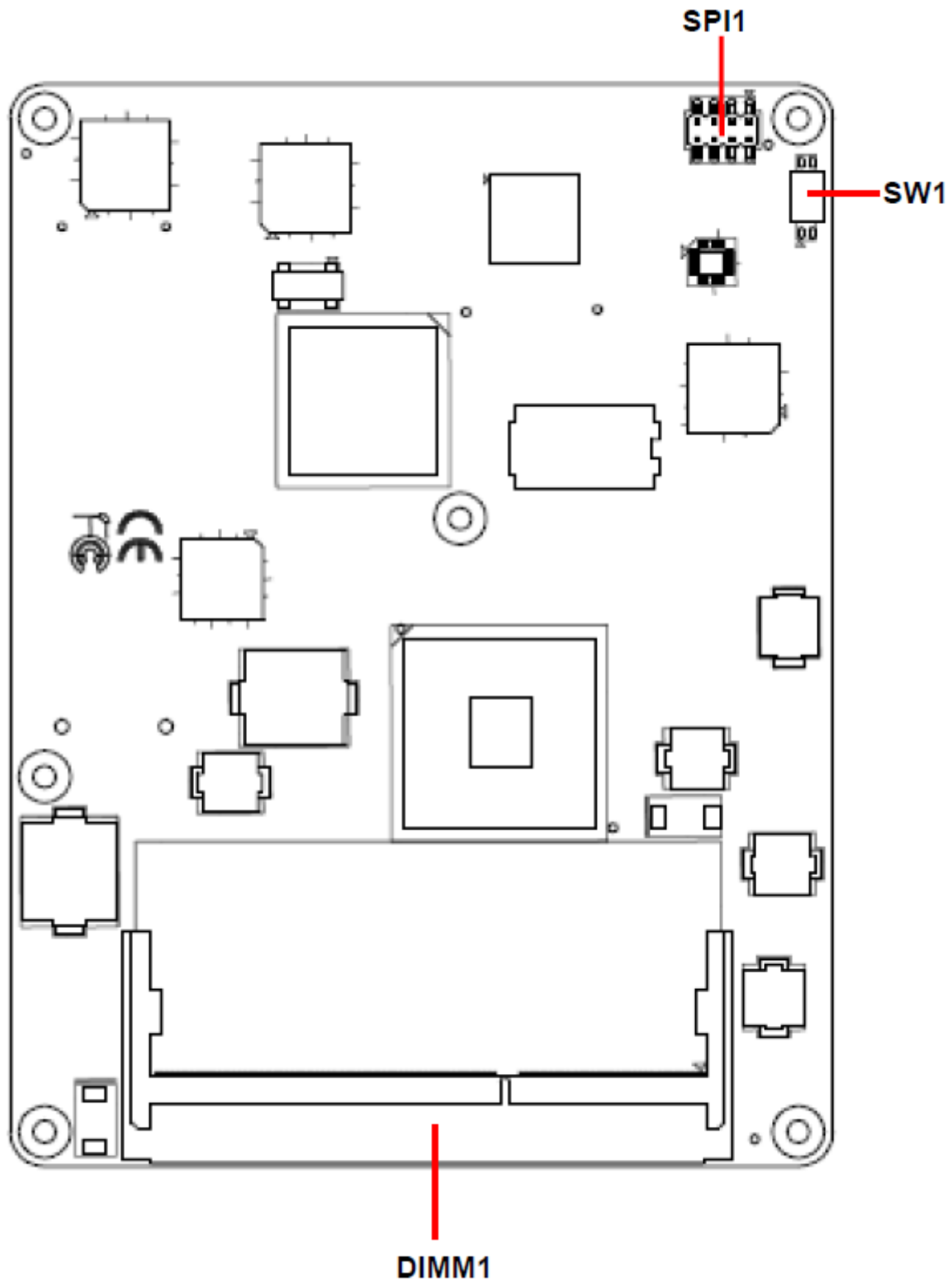
- 1 x ESM-CDV COM Express Module
- 1 x Quick Installation Guide
- 1 x DVD-ROM contains the followings:
 - User's Manual (this manual in PDF file)
 - Chipset and Ethernet driver

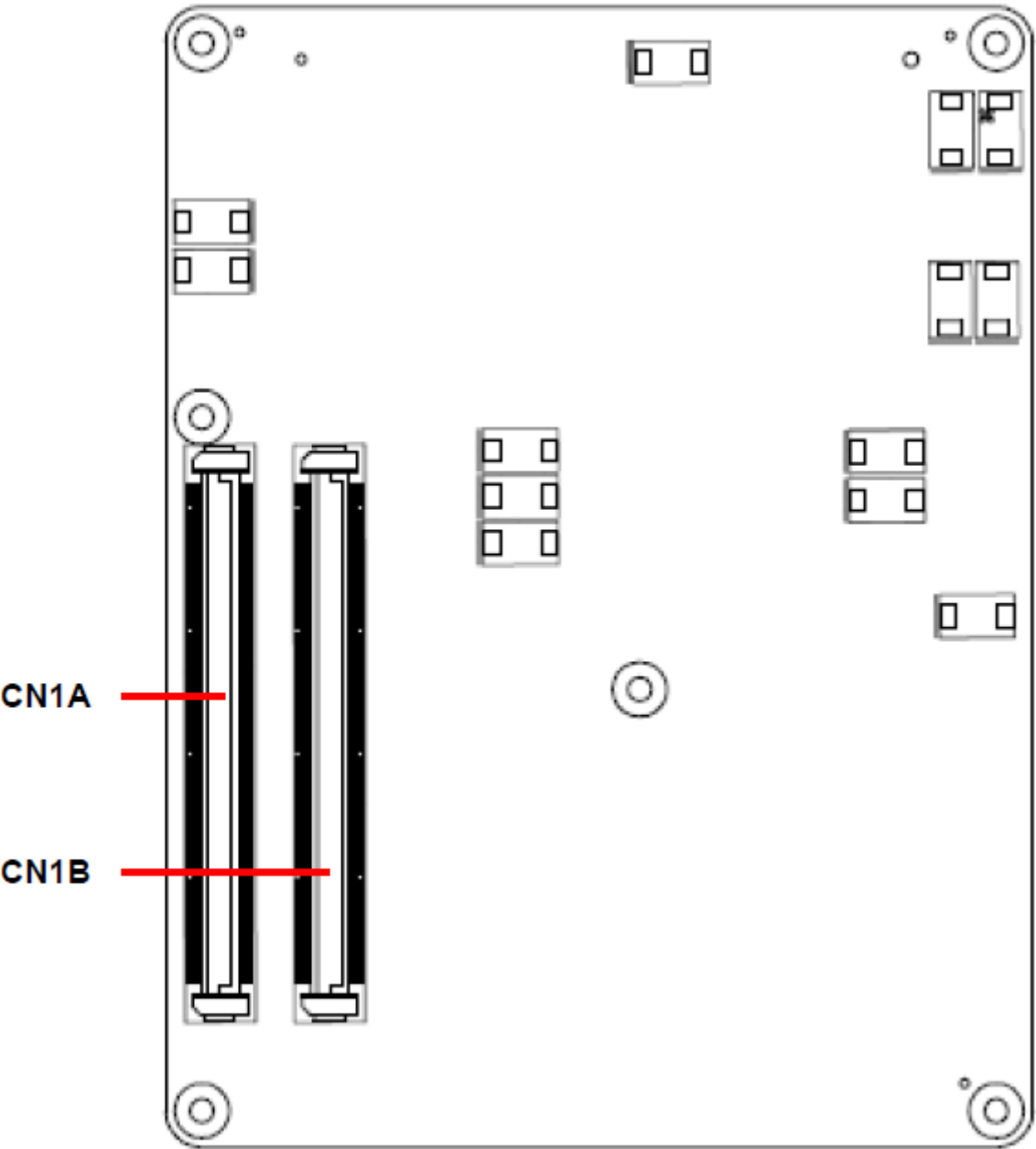


If any of the above items is damaged or missing, contact your retailer.

2. Hardware Configuration

2.1 Product Overview

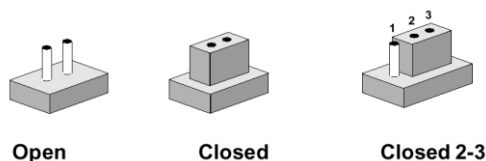




2.2 Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:



A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

The following tables list the function of each of the board’s jumpers and connectors.

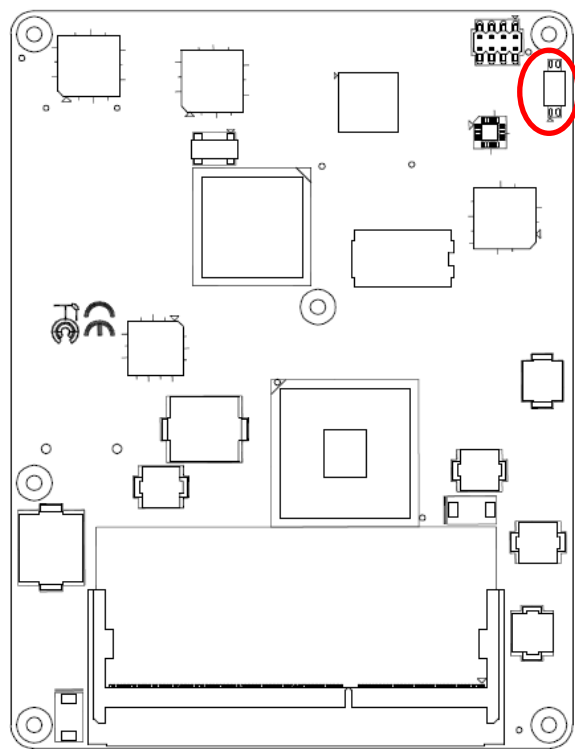
Connectors

Label	Function	Note
SPI1	(Reserved for BIOS programming)	4 x 2 header, pitch 2.0mm
CN1A	COM Express connector 1	
CN1B	COM Express connector 2	
DIMM1	204-pin DDR3 SDRAM DIMM socket	
SW1	AT/ATX mode selector	

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2.3 Setting Jumpers & Connectors

2.3.1 AT/ATX mode selector (SW1)

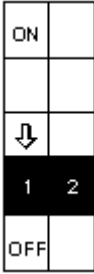
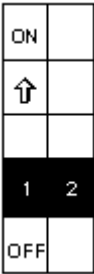


*Default



AT/ATX mode



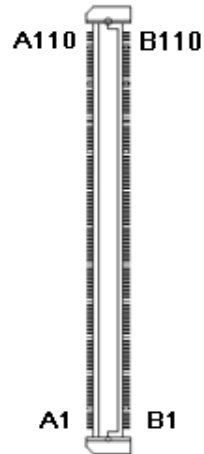
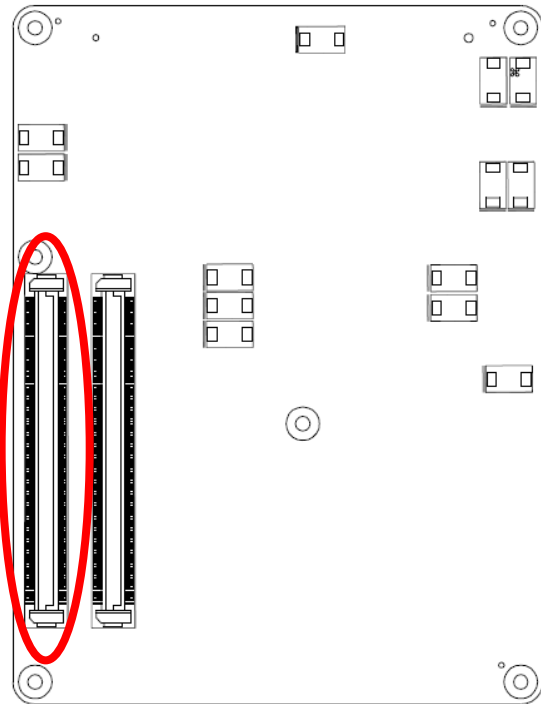
AT mode ATX mode*



2.3.1.1 Signal Description –AT/ATX mode selection

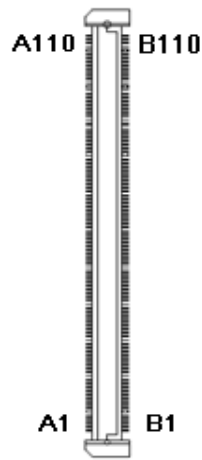
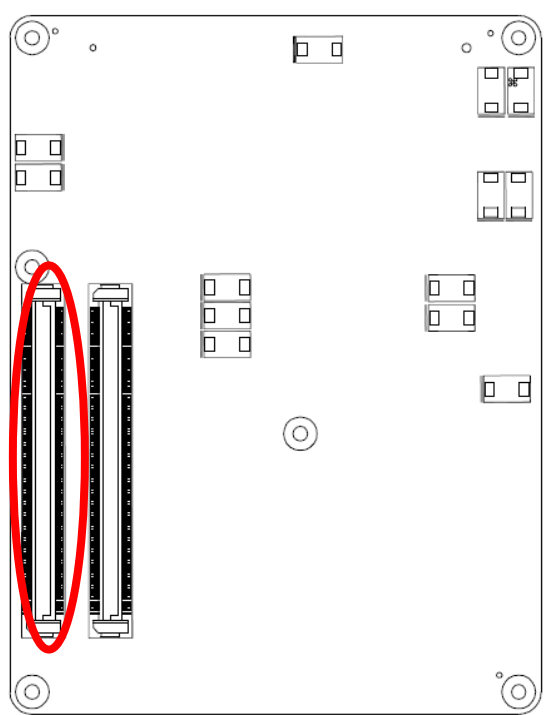
AT/ATX mode	Description
<p>AT mode</p> 	<p>This Mode supports AT power supply, no need to press Power button to enable power on/off</p>
<p>ATX mode</p> 	<p>This Mode supports ATX power supply. Press the ATX power button to enable power on/off</p>

2.3.2 COM Express Connector 1 (CN1A)



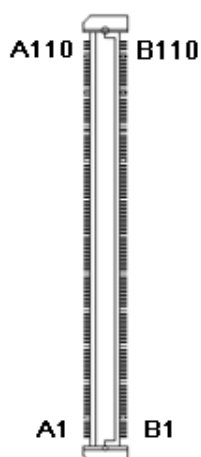
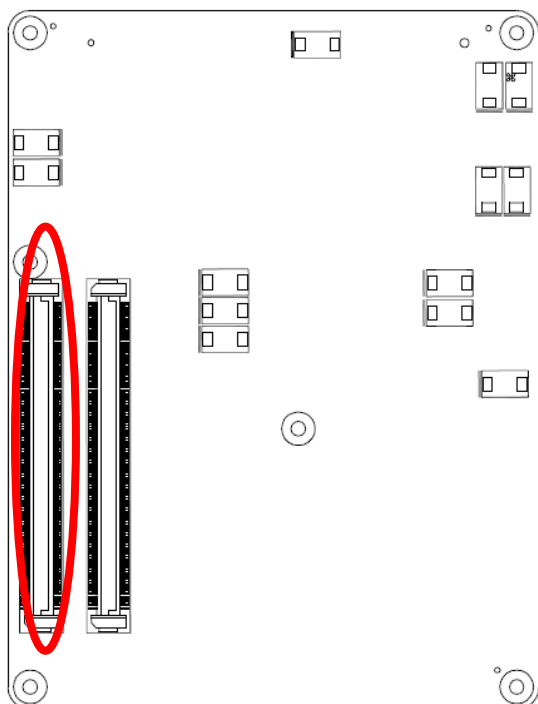
Signal	PIN	PIN	Signal
GND	A1	B1	GND
GBE0_MDI3-	A2	B2	GBE0_ACT#
GBE0_MDI3+	A3	B3	LPC_FRAME#
GBE0_LINK100#	A4	B4	LPC_AD0
GBE0_LINK1000#	A5	B5	LPC_AD1
GBE0_MDI2-	A6	B6	LPC_AD2
GBE0_MDI2+	A7	B7	LPC_AD3
GBE0_LINK#	A8	B8	LPC_DRQ0#
GBE0_MDI1-	A9	B9	LPC_DRQ1#
GBE0_MDI1+	A10	B10	LPC_CLK
GND	A11	B11	GND
GBE0_MDI0-	A12	B12	PWRBTN#
GBE0_MDI0+	A13	B13	SMB_CK
GBE0_CTREF	A14	B14	SMB_DAT
SUS_S3#	A15	B15	SMB_ALERT#
SATA0_TX+	A16	B16	SATA1_TX+
SATA0_TX-	A17	B17	SATA1_TX-
SUS_S4#	A18	B18	SUS_STAT#
SATA0_RX+	A19	B19	SATA1_RX+
SATA0_RX-	A20	B20	SATA1_RX-
GND	A21	B21	GND
NC	A22	B22	NC
NC	A23	B23	NC
SUS_S5#	A24	B24	PWR_OK
NC	A25	B25	NC
NC	A26	B26	NC
BATLOW#	A27	B27	WDT
ATA_ACT#	A28	B28	AC_SDIN2
AC_SYNC	A29	B29	AC_SDIN1
AC_RST#	A30	B30	AC_SDIN0

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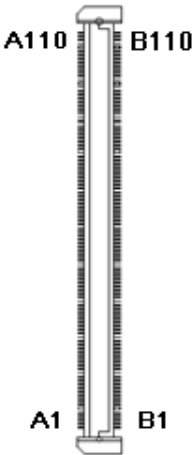
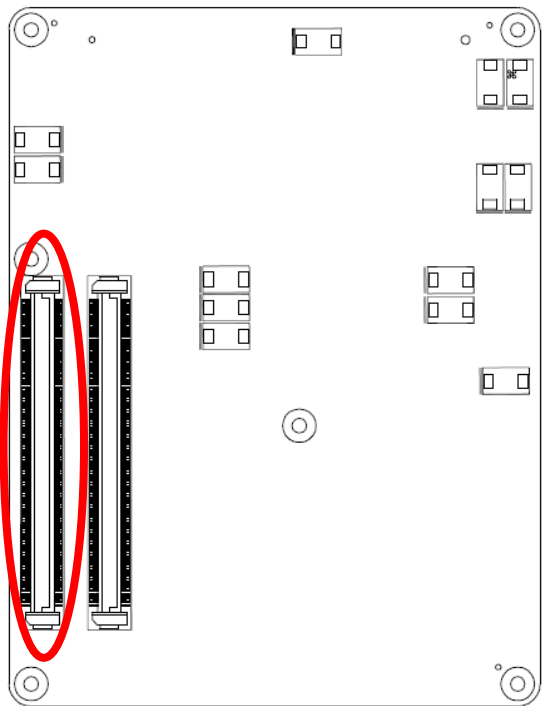
Signal	PIN	PIN	Signal
GND	A31	B31	GND
AC_BITCLK	A32	B32	SPKR
AC_SDOUT	A33	B33	I2C_CK
BIOS_DISABLE#	A34	B34	I2C_DAT
THRMTRIP#	A35	B35	THRM#
USB6-	A36	B36	USB7-
USB6+	A37	B37	USB7+
USB_6_7_OC#	A38	B38	USB_4_5_OC#
USB4-	A39	B39	USB5-
USB4+	A40	B40	USB5+
GND	A41	B41	GND
USB2-	A42	B42	USB3-
USB2+	A43	B43	USB3+
USB_2_3_OC#	A44	B44	USB_0_1_OC#
USB0-	A45	B45	USB1-
USB0+	A46	B46	USB1+
VCC_RTC	A47	B47	EXCD1_PERST#
EXCD0_PERST#	A48	B48	EXCD1_CPPE#
EXCD0_CPPE#	A49	B49	SYS_RESET#
LPC_SERIRQ	A50	B50	CB_RESET#
GND	A51	B51	GND
NC	A52	B52	NC
NC	A53	B53	NC
GPI0	A54	B54	GPO1
NC	A55	B55	NC
NC	A56	B56	NC
GND	A57	B57	GPO2
PCIE_TX3+	A58	B58	PCIE_RX3+
PCIE_TX3-	A59	B59	PCIE_RX3-
GND	A60	B60	GND

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Signal	PIN	PIN	Signal
PCIE_TX2+	A61	B61	PCIE_RX2+
PCIE_TX2-	A62	B62	PCIE_RX2-
GPI1	A63	B63	GPO3
PCIE_TX1+	A64	B64	PCIE_RX1+
PCIE_TX1-	A65	B65	PCIE_RX1-
GND	A66	B66	WAKE0#
GPI2	A67	B67	WAKE1#
PCIE_TX0+	A68	B68	PCIE_RX0+
PCIE_TX0-	A69	B69	PCIE_RX0-
GND	A70	B70	GND
LVDS_A0+	A71	B71	LVDS_B0+
LVDS_A0-	A72	B72	LVDS_B0-
LVDS_A1+	A73	B73	LVDS_B1+
LVDS_A1-	A74	B74	LVDS_B1-
LVDS_A2+	A75	B75	LVDS_B2+
LVDS_A2-	A76	B76	LVDS_B2-
LVDS_VDD_EN	A77	B77	LVDS_B3+
LVDS_A3+	A78	B78	LVDS_B3-
LVDS_A3-	A79	B79	LVDS_BKLT_EN
GND	A80	B80	GND
LVDS_A_CK+	A81	B81	LVDS_B_CK+
LVDS_A_CK-	A82	B82	LVDS_B_CK-
LVDS_I2C_CK	A83	B83	LVDS_BKLT_CTRL
LVDS_I2C_DAT	A84	B84	VCC_5V_SBY_1
GPI3	A85	B85	VCC_5V_SBY_2
KBD_RST#	A86	B86	VCC_5V_SBY_3
KBD_A20GATE	A87	B87	VCC_5V_SBY_4
PCIE_CK_REF0+	A88	B88	RSVD5
PCIE_CK_REF0--	A89	B89	VGA_RED
GND	A90	B90	GND

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Signal	PIN	PIN	Signal
RSVD1	A91	B91	VGA_GRN
RSVD2	A92	B92	VGA_BLU
GPO0	A93	B93	VGA_HSYNC
RSVD3	A94	B94	VGA_VSYNC
RSVD4	A95	B95	VGA_I2C_CK
GND	A96	B96	VGA_I2C_DAT
NC	A97	B97	SPI_CS#
NC	A98	B98	NC
NC	A99	B99	NC
GND	A100	B100	GND
NC	A101	B101	NC
NC	A102	B102	NC
NC	A103	B103	NC
VCC_12V	A104	B104	VCC_12V
VCC_12V	A105	B105	VCC_12V
VCC_12V	A106	B106	VCC_12V
VCC_12V	A107	B107	VCC_12V
VCC_12V	A108	B108	VCC_12V
VCC_12V	A109	B109	VCC_12V
GND	A110	B110	GND

2.3.2.1 Signal Description – COM Express Connector 1 (CN1A)

2.3.2.1.1 Audio Signals

Signal	Signal Description
AC_SYNC	HD Audio Sync
AC_RST#	HD Audio Reset
AC_SDIN[0:2]	Audio CODEC Serial Data
AC_BITCLK	HD Audio Clock
AC_SDOUT	HD Audio Data

2.3.2.1.2 Gigabit Ethernet Signals

Signal	Signal Description			
GBE0_MD[0:3] +/-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:			
		1000B-T	100B-T	10B-T
	MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
	MDI[1]+/	B1_DB+/-	RX+/-	RX+/-
	MDI[2]+/	B1_DC+/-	X	X
	MDI[3]+/	B1_DD+/-	X	X
GBE0_ACT#	Gigabit Ethernet Controller 0 activity indicator, active low.			
GBE0_Link#	Gigabit Ethernet Controller 0 link indicator, active low.			
GBE0_Link100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.			
GBE0_Lin1000#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.			

2.3.2.1.3 GPIO Signals

Signal	Signal Description
GPI[0:4]	General purpose input pins.
GPO[0:4]	General purpose output pins.

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2.3.2.1.4 Flat Panel LVDS Signals

Signal	Signal Description
BIASON	Controls panel contrast voltage.
DIGON	Controls panel digital power.
ENBKL#	Controls backlight power enable.
I ² C_DAT, I ² C_CLK	I ² C interface for panel parameter EEPROM. This EEPROM is mounted on the LVDS receiver. The data in the EEPROM allows the EXT module to automatically set the proper timing parameters for a specific LCD panel.

2.3.2.1.5 LPC Signals

Signal	Signal Description
LPC_FRAME#	LPC frame indicates the start of an LPC cycle
LPC_AD[0:3]	LPC multiplexed address, command and data bus
LPC_DRQ[0:1]#	LPC serial DMA request
LPC_CLK	LPC clock output - 33MHz nominal
LPC_SERIRQ	LPC serial interrupt

2.3.2.1.6 Miscellaneous Signals

Signal	Signal Description							
I ² C_CLK	General purpose I ² C port clock output							
I ² C_DAT	General purpose I ² C port data I/O line							
SPKR	Output for audio enunciator - the "speaker" in PC-AT systems							
KBD_RST#	Input to Module from (optional) external keyboard controller that can force a reset.							
KBD_A20GATE	Input to Module from (optional) external keyboard controller that can be used to control the CPU A20 gate line.							
BIOS_DIS0# BIOS_DIS1#	Selection straps to determine the BIOS boot device							
	BIOS_DIS1#	BIOS_DIS0#	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	Ref Line
	1	1	Module	Module	High	Module	SPI0/SPI1	0
	1	0	Module	Module	High	Module	Carrier FWH	1
	0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
	0	0	Carrier	Module	SPI1	Module	SPI0/SPI1	3
KB_RST#	Input to module from (optional) external keyboard controller that can force a reset.							
KB_A20GATE	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line.							

2.3.2.1.7 PCI Express Signals

Signal	Signal Description
PCIE_TX[0:3] +/-	PCI Express Differential Transmit Pair 0-3
PCIE_RX[0:3] +/-	PCI Express Differential Receive Pair 0-3
PCIE0_CK_REF+/-	Reference clock output for PCI Express lanes 0-7 and for PCI Express Graphics lanes 0-15

2.3.2.1.8 Power Signals

Signal	Signal Description
VCC_5V_SBY	Standby power input: +5.0V nominal. See Electrical Specifications for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) must be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.
VCC_RTC	Real-time clock circuit-power input. Nominally +3.0V.

2.3.2.1.9 Power & System Management Signals

Signal	Signal Description
SUS_S3#	Indicates system is in Suspend to RAM state. Active low output.
SUS_S4#	Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	Indicates system is in Soft Off state.
BATLOW#	Indicates that external battery is low
PWRBTN#	Power button to bring system out of S5 (soft off), active on rising edge.
SMB_CK	System Management Bus bidirectional clock line.
SMB_DTA	System Management Bus bidirectional data line.
SMB_ALERT#	System Management Bus Alert - input can be used to generate an SMI# (System Management Interrupt) or to wake the system.
SUS_STAT#	Indicates imminent suspend operation.
PWR_OK	Power OK from main power supply
THRMTRIP#	Active low output indicating that the CPU has entered thermal shutdown.
THRM#	Input from off-module temp sensor indicating and over-temp situation.
SYS_RESET#	Reset button input. Active low input.
WAKE0#	PCI Express wake up signal.
WAKE1#	General purpose wake up signal.

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2.3.2.1.10 SATA Signals

Signal	Signal Description
SATA[0:1]_TX +/-	Serial ATA Channel 0-1 transmit differential pair.
SATA[0:1]_RX +/-	Serial ATA Channel 0-1 receive differential pair.
ATA_ACT#	ATA (parallel and serial) activity indicator, active low.

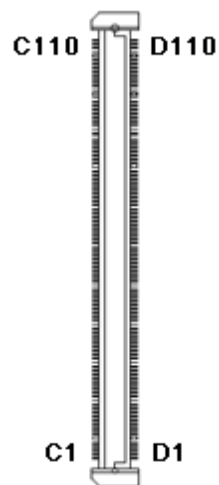
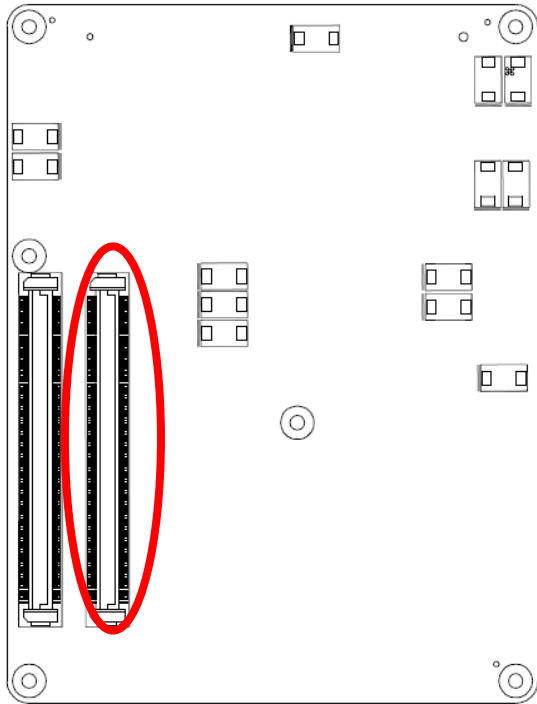
2.3.2.1.11 VGA Signals

Signal	Signal Description
VGA_RED	Red for monitor. Analog DAC output.
VGA_GRN	Green for monitor. Analog DAC output.
VGA_BLU	Blue for monitor. Analog DAC output.
VGA_HSYNC	Horizontal sync output to VGA monitor
VGA_VSYNC	Vertical sync output to VGA monitor
VGA_I ² C_CK	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)
VGA_I ² C_DAT	DDC data line.

2.3.2.1.12 USB Signals

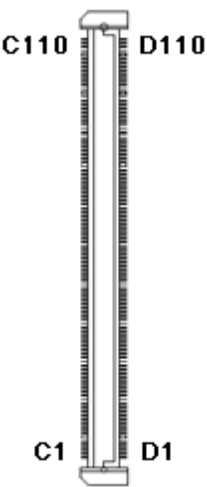
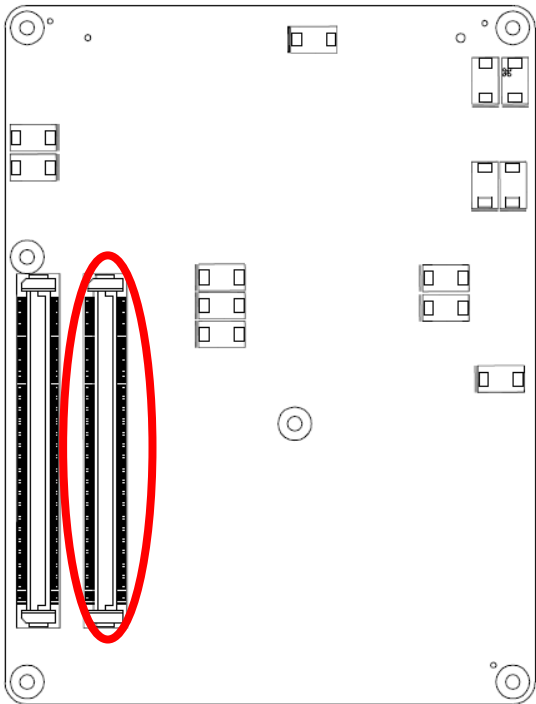
Signal	Signal Description
USB[0:7] +/-	USB differential pairs, channels 0 through 7
USB_0_1_OC#	USB over-current sense, USB channels 0 and 1
USB_2_3_OC#	USB over-current sense, USB channels 2 and 3
USB_4_5_OC#	USB over-current sense, USB channels 4 and 5
USB_6_7_OC#	USB over-current sense, USB channels 6 and 7

2.3.3 COM Express Connector 2 (CN1B)



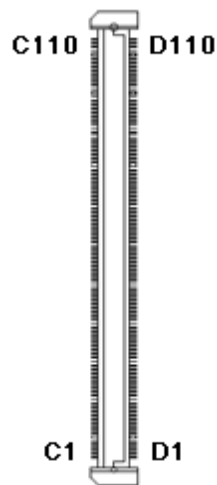
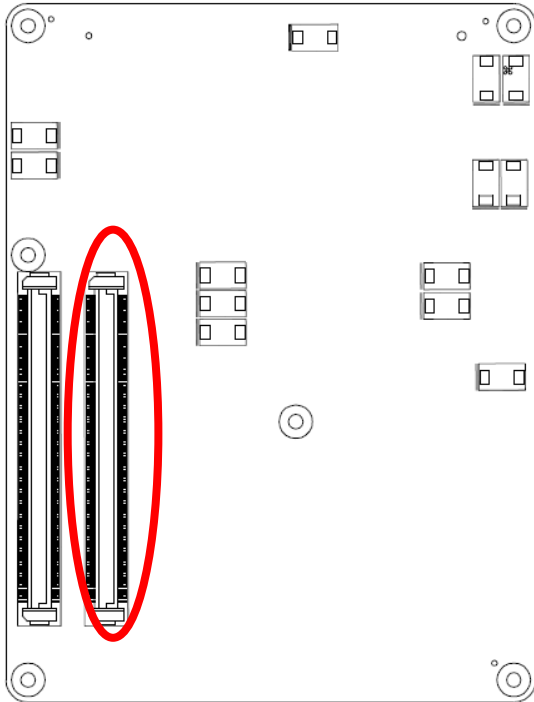
Signal	PIN	PIN	Signal
GND	C1	D1	GND
IDE_D7	C2	D2	IDE_D5
IDE_D6	C3	D3	IDE_D10
IDE_D3	C4	D4	IDE_D11
IDE_D15	C5	D5	IDE_D12
IDE_D8	C6	D6	IDE_D4
IDE_D9	C7	D7	IDE_D0
IDE_D2	C8	D8	IDE_REQ
IDE_D13	C9	D9	IDE_IOW#
IDE_D1	C10	D10	IDE_ACK#
GND	C11	D11	GND
IDE_D14	C12	D12	IDE_IRQ
IDE_IORDY	C13	D13	IDE_A0
IDE_IOR#	C14	D14	IDE_A1
PCI_PME#	C15	D15	IDE_A2
NC	C16	D16	IDE_CS1#
NC	C17	D17	IDE_CS3#
PCI_GNT1#	C18	D18	IDE_RESET#
PCI_REQ1#	C19	D19	NC
PCI_GNT0#	C20	D20	NC
GND	C21	D21	GND
PCI_REQ0#	C22	D22	PCI_AD1
PCI_RESET#	C23	D23	PCI_AD3
PCI_AD0	C24	D24	PCI_AD5
PCI_AD2	C25	D25	PCI_AD7
PCI_AD4	C26	D26	PCI_C/BE0#
PCI_AD6	C27	D27	PCI_AD9
PCI_AD8	C28	D28	PCI_AD11
PCI_AD10	C29	D29	PCI_AD13
PCI_AD12	C30	D30	PCI_AD15

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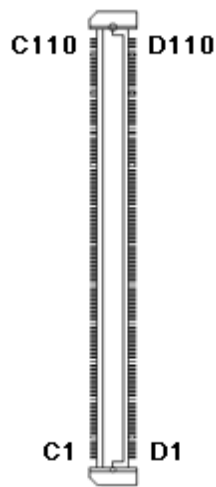
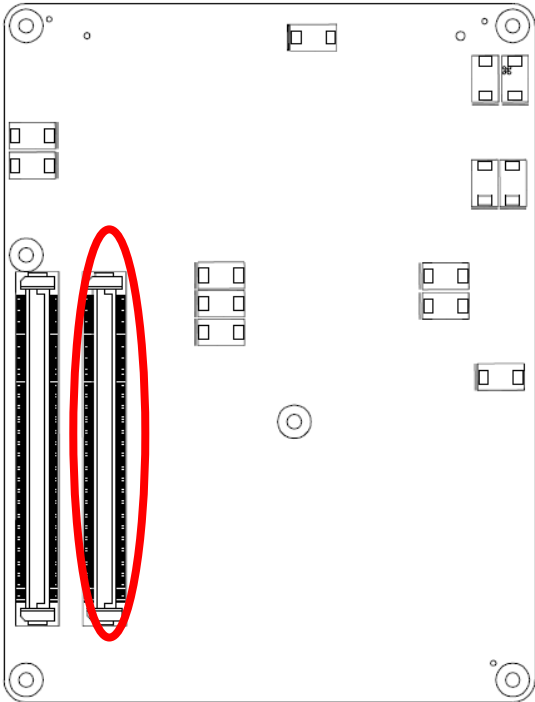
Signal	PIN	PIN	Signal
GND	C31	D31	GND
PCI_AD14	C32	D32	PCI_PAR
PCI_C/BE1#	C33	D33	PCI_SERR#
PCI_PERR#	C34	D34	PCI_STOP#
PCI_LOCK#	C35	D35	PCI_TRDY#
PCI_DEVSEL#	C36	D36	PCI_FRAME#
PCI_IRDY#	C37	D37	PCI_AD16
PCI_C/BE2#	C38	D38	PCI_AD18
PCI_AD17	C39	D39	PCI_AD20
PCI_AD19	C40	D40	PCI_AD22
GND	C41	D41	GND
PCI_AD21	C42	D42	PCI_AD24
PCI_AD23	C43	D43	PCI_AD26
PCI_C/BE3#	C44	D44	PCI_AD28
PCI_AD25	C45	D45	PCI_AD30
PCI_AD27	C46	D46	PCI_IRQC#
PCI_AD29	C47	D47	PCI_IRQD#
PCI_AD31	C48	D48	PCI_CLKRUN#
PCI_IRQA#	C49	D49	NC
PCI_IRQB#	C50	D50	PCI_CLK
GND	C51	D51	GND
NC	C52	D52	NC
NC	C53	D53	NC
NC	C54	D54	NC
NC	C55	D55	NC
NC	C56	D56	NC
NC	C57	D57	NC
NC	C58	D58	NC
NC	C59	D59	NC
GND	C60	D60	GND

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Signal	PIN	PIN	Signal
NC	C61	D61	NC
NC	C62	D62	NC
NC	C63	D63	NC
NC	C64	D64	NC-
NC	C65	D65	NC
NC	C66	D66	NC
NC	C67	D67	GND
NC	C68	D68	NC
NC	C69	D69	NC
GND	C70	D70	GND
NC	C71	D71	NC
NC	C72	D72	NC
NC	C73	D73	NC
NC	C74	D74	NC
NC	C75	D75	NC
GND	C76	D76	GND
NC	C77	D77	IDE_CBLID#
NC	C78	D78	NC
NC	C79	D79	NC
GND	C80	D80	GND
NC	C81	D81	NC
NC	C82	D82	NC
NC	C83	D83	NC
GND	C84	D84	GND
NC	C85	D85	NC
NC	C86	D86	NC
GND	C87	D87	GND
NC	C88	D88	NC
NC	C89	D89	NC
GND	C90	D90	GND

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Signal	PIN	PIN	Signal
NC	C91	D91	NC
NC	C92	D92	NC
GND	C93	D93	GND
NC	C94	D94	NC
NC	C95	D95	NC
GND	C96	D96	GND
NC	C97	D97	NC
NC	C98	D98	NC
NC	C99	D99	NC
GND	C100	D100	GND
NC	C101	D101	NC
NC	C102	D102	NC
GND	C103	D103	GND
VCC_12V	C104	D104	VCC_12V
VCC_12V	C105	D105	VCC_12V
VCC_12V	C106	D106	VCC_12V
VCC_12V	C107	D107	VCC_12V
VCC_12V	C108	D108	VCC_12V
VCC_12V	C109	D109	VCC_12V
GND	C110	D110	GND

2.3.3.1 Signal Description – COM Express Connector 2 (CN1B)

2.3.3.1.1 PCI Signals

Signal	Signal Description
PCI_AD[0:31]	PCI bus multiplexed address and data lines.
PCI_C/BE[0:3]#	PCI bus byte enable lines, active low.
PCI_DEVSEL#	PCI bus Device Select, active low.
PCI_FRAME#	PCI bus Frame control line, active low.
PCI_IRDY#	PCI bus Initiator Ready control line, active low.
PCI_TRDY#	PCI bus Target Ready control line, active low.
PCI_STOP#	PCI bus STOP control line, active low, driven by cycle initiator.
PCI_PAR	PCI bus parity.
PCI_PERR#	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.
PCI_REQ[0:3]#	PCI bus master request input lines, active low.
PCI_GNT[0:3]#	PCI bus master grant output lines, active low.
PCI_RESET#	PCI Reset output, active low.
PCI_LOCK#	PCI Lock control line, active low.
PCI_SERR#	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.
PCI_PME#	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1-S5.
PCI_CLKRUN#	Bidirectional pin used to support PCI clock run protocol for mobile systems.
PCI_IRQ[A:D]#	PCI interrupt request lines.
PCI_CLK	PCI 33MHz clock output.

2.3.3.1.2 IDE Signals

Signal	Signal Description
IDE_D[0:15]	Bidirectional data to / from IDE device.
IDE_A[0:2]	Address lines to IDE device.
IDE_LOW#	I/O write line to IDE device. Data latched on trailing (rising) edge.
IDE_IOR#	I/O read line to IDE device.
IDE_REQ	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.
IDE_ACK#	IDE Device DMA Acknowledge.

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IDE_CS1#	IDE Device Chip Select for 1F0h to 1FFh range.
IDE_CS3#	IDE Device Chip Select for 3F0h to 3FFh range.
IDE_IORDY	IDE device I/O ready input Pulled low by the IDE device to extend the cycle.
IDE_RESET#	Reset output to IDE device, active low.
IDE_IRQ	Interrupt request from IDE device.
IDE_CBLID#	Input from off-Module hardware indicating the type of IDE cable being used.

