ESM-QM57

Intel Core i7/ Celeron COM Express Module

Quick Installation Guide

1st Ed –6 April 2011

Notice

This guide is designed for experienced users to perform quick setup of the system. For detailed information, please always refer to the electronic user's manual.

Copyright Notice

Part No. E2017286001R

1. Getting Started

1.1 Safety Precautions

Warning!

Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!

Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

1.2 Packing List

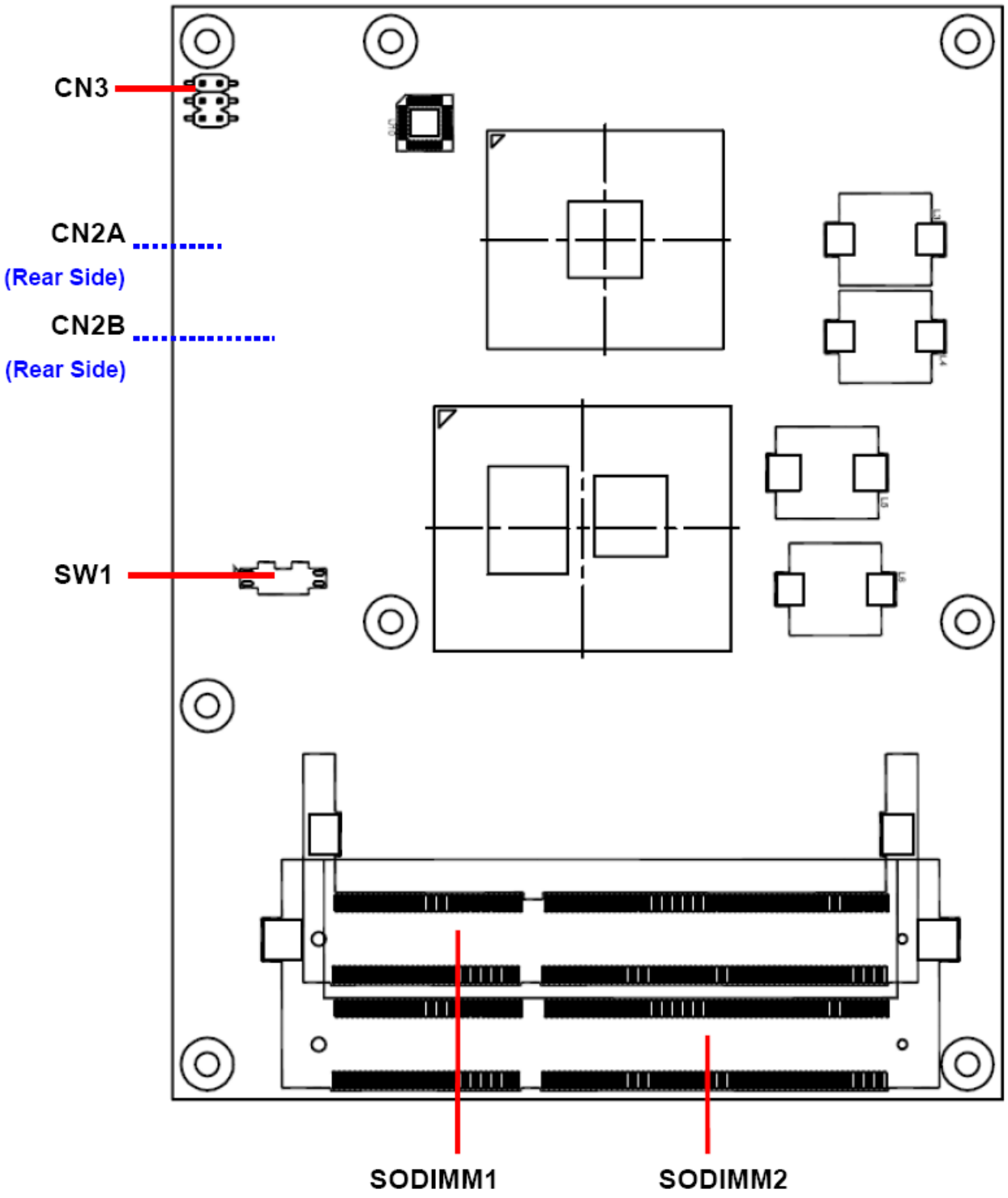
Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 x ESM-QM57 Intel Core i7/ Celeron COM Express Module
- 1 x Quick Installation Guide
- 1 x DVD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Chipset and Ethernet driver

If any of the above items is damaged or missing, contact your retailer.

2. Hardware Configuration

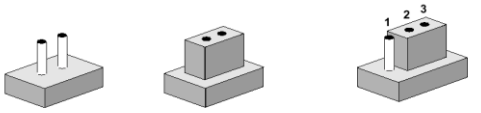
2.1 Product Overview



2.2 Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



Open Closed Closed 2-3

The jumper settings are schematically depicted in this manual as follows:

Open Closed Closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

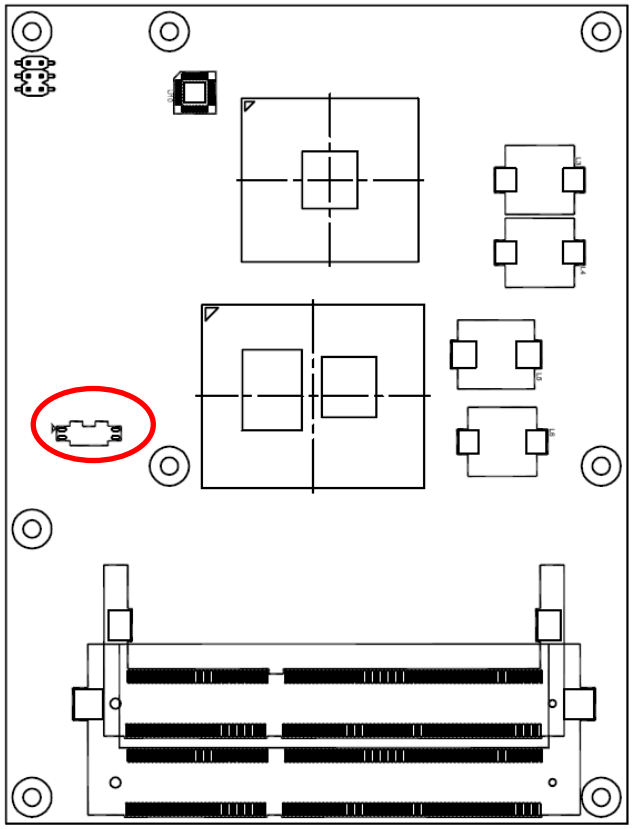
The following tables list the function of each of the board’s jumpers and connectors.

Connectors

Label	Function	Note
CN3	(Reserved for BIOS programming)	3 x 2 header, pitch 2.0mm
CN2A	COM Express connector 1	
CN2B	COM Express connector 2	
SODIMM1	204-pin DDR3 SDRAM DIMM socket	
SODIMM2	204-pin DDR3 SDRAM DIMM socket	
SW1	AT/ATX mode selector	

2.3 Setting Jumpers & Connectors

2.3.1 AT/ATX mode selector (SW1)



AT/ATX mode

AT mode

OFF	1		⇨	ON
	2			

ATX mode*

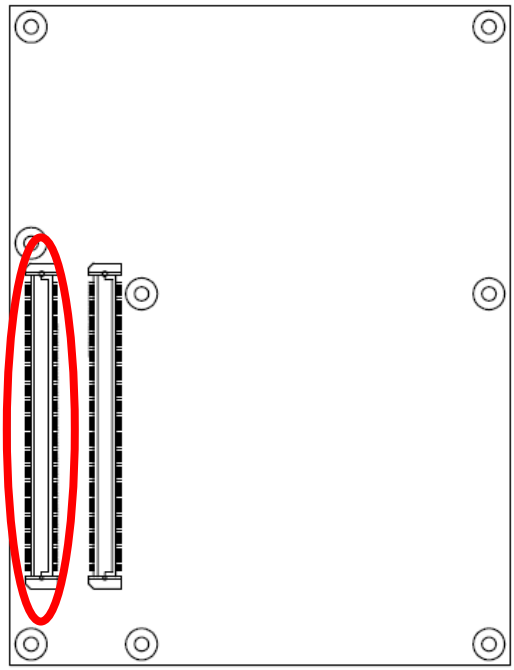
OFF	1	⇦		ON
	2			

***Default**

2.3.1.1 Signal Description –AT/ATX mode selection

AT/ATX mode	Description
AT mode 	This Mode supports AT power supply, no need to press Power button to enable power on/off
ATX mode 	This Mode supports ATX power supply. Press the ATX power button to enable power on/off

2.3.2 COM Express Connector 1 (CN2A)



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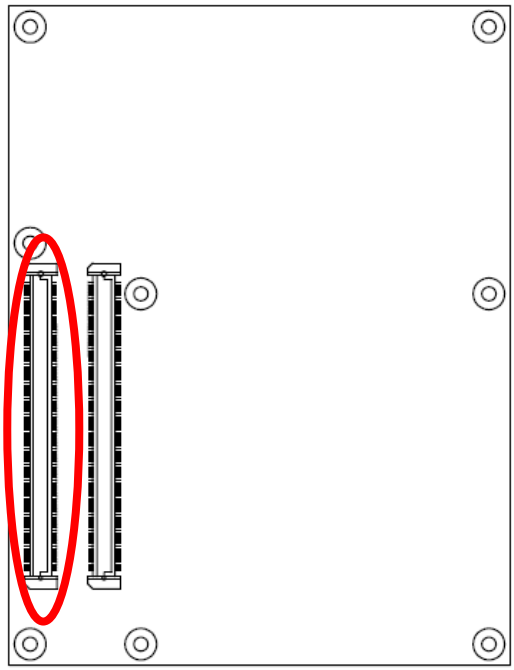
Signal	PIN	PIN	Signal
GND	A1	B1	GND
PCIE_MDI3-	A2	B2	PCIE_ACT#
PCIE_MDI3+	A3	B3	LPC_FRAME#
PCIE_LINK100#	A4	B4	LPC_AD0
PCIE_LINK1000#	A5	B5	LPC_AD1
PCIE_MDI2-	A6	B6	LPC_AD2
PCIE_MDI2+	A7	B7	LPC_AD3
PCIE_LINK#	A8	B8	LPC_DRQ0#
PCIE_MDI1-	A9	B9	LPC_DRQ1#
PCIE_MDI1+	A10	B10	CLK_LPC_33M
GND	A11	B11	GND
PCIE_MDI0-	A12	B12	PWRBTN#
PCIE_MDI0+	A13	B13	SMB_CLK
LAN_1.9V	A14	B14	SMB_DATA
SLP_S3#	A15	B15	LINKALERT#
SATAP0_TXP	A16	B16	SATAP1_TXP
SATAP0_TXN	A17	B17	SATAP1_TXN
SLP_S4#	A18	B18	PM_SUS_SATA#
SATAP0_RXP	A19	B19	SATAP1_RXP
SATAP0_RXN	A20	B20	SATAP1_RXN
GND	A21	B21	GND
SATAP2_TXP	A22	B22	SATAP3_TXP
SATAP2_TXN	A23	B23	SATAP3_TXN
SLP_S5#	A24	B24	POWER_OK
SATAP2_RXP	A25	B25	SATAP3_PXP
SATAP2_RXN	A26	B26	SATAP3_PXN
PM_BATLOW#	A27	B27	WDT
SATA_LED#	A28	B28	HAD_SDIN2
HAD_SYNC	A29	B29	HAD_SDIN1
HAD_RST#	A30	B30	HAD_SDIN0



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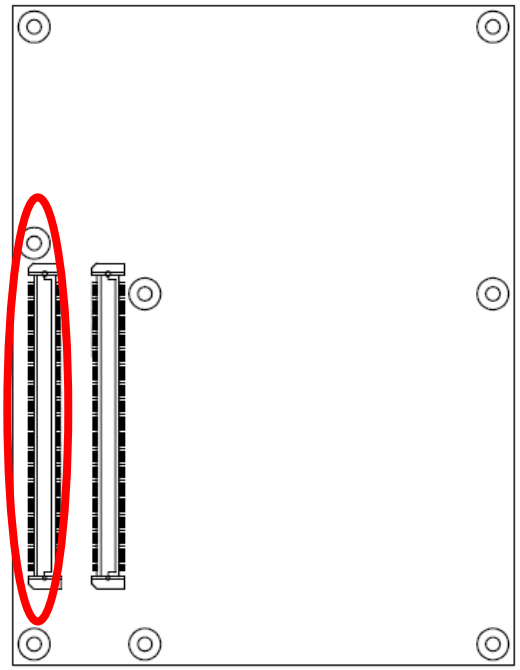
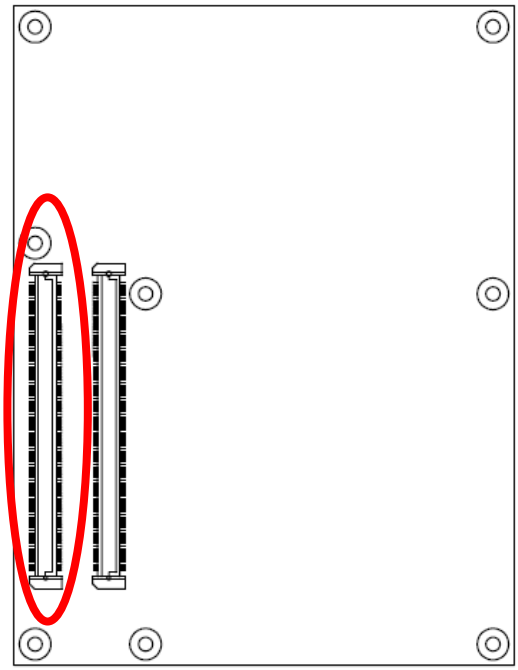
Signal	PIN	PIN	Signal
GND	A31	B31	GND
HAD_BIT_CLK	A32	B32	HAD_SPKR
HAD_SDOUT	A33	B33	I2C_CLK
BIOS_DISABLE#	A34	B34	I2C_DAT
PM_THRMTRIP#	A35	B35	ETX_THRM#
USB_PN6	A36	B36	USB_PN7
USB_PP6	A37	B37	USB_PP7
USB_OC67#	A38	B38	USB_OC45#
USB_PN4	A39	B39	USB_PN5
USB_PP4	A40	B40	USB_PP5
GND	A41	B41	GND
USB_PN2	A42	B42	USB_PN3
USB_PP2	A43	B43	USB_PP3
USB_OC23#	A44	B44	USB_OC01#
USB_PN0	A45	B45	USB_PN1
USB_PP0	A46	B46	USB_PP1
RTC_VCC	A47	B47	PLTRST#
PLTRST#	A48	B48	EXCD1_CPPE#
EXCD0_CPPE#	A49	B49	PM_SYSRST#
PCI_SERIRQ	A50	B50	BU_PLTRST#
GND	A51	B51	GND
PCIE8_TX+	A52	B52	PCIE8_RX+
PCIE8_TX-	A53	B53	PCIE8_RX-
ETX_GPIO43	A54	B54	ETX_GPIO10
PCIE7_TX+	A55	B55	PCIE7_RX+
PCIE7_TX-	A56	B56	PCIE7_RX-
GND	A57	B57	ETX_GPIO2
PCIE4_TX+	A58	B58	PCIE4_RX+
PCIE4_TX-	A59	B59	PCIE4_RX-
GND	A60	B60	GND



(Rear side)

Signal	PIN	PIN	Signal
PCIE3_TX+	A61	B61	PCIE3_RX+
PCIE3_TX-	A62	B62	PCIE3_RX-
ETX_GPIO45	A63	B63	ETX_GPIO15
PCIE2_TX+	A64	B64	PCIE2_RX+
PCIE2_TX-	A65	B65	PCIE2_RX-
GND	A66	B66	PCIE_WAKE#
ETX_GPIO46	A67	B67	PM_RI#
PCIE1_TX+	A68	B68	PCIE1_RX+
PCIE1_TX-	A69	B69	PCIE1_RX-
GND	A70	B70	GND
LVDSA_DATA0	A71	B71	LVDSB_DATA0
LVDSA_DATA#0	A72	B72	LVDSB_DATA#0
LVDSA_DATA1	A73	B73	LVDSB_DATA1
LVDSA_DATA#1	A74	B74	LVDSB_DATA#1
LVDSA_DATA2	A75	B75	LVDSB_DATA2
LVDSA_DATA#2	A76	B76	LVDSB_DATA#2
LVDS_VDD_EN	A77	B77	LVDSB_DATA3
LVDSA_DATA3	A78	B78	LVDSB_DATA#3
LVDSA_DATA#3	A79	B79	LVDS_BKLT_EN
GND	A80	B80	GND
LVDSA_CLK	A81	B81	LVDSB_CLK
LVDSA_CLK#	A82	B82	LVDSB_CLK#
LVDS_DDC_CLK	A83	B83	LVDS_BKLT_CTRL
LVDS_DDC_DATA	A84	B84	5VSB
ETX_GPIO7	A85	B85	5VSB
KBRST#	A86	B86	5VSB
H_A20GATE	A87	B87	5VSB
CLK_PCIE_ETX+	A88	B88	NC
CLK_PCIE_ETX-	A89	B89	CRT_RED
GND	A90	B90	GND



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Signal	PIN	PIN	Signal
CLK_PEG_A+	A91	B91	CRT_GREEN
CLK_PEG_A-	A92	B92	CRT_BLUE
ETX_GPIO09	A93	B93	CRT_HSYNC
GPIO06	A94	B94	CRT_VSYNC
GPIO07	A95	B95	CRT_DDC_CLK
GND	A96	B96	CRT_DDC_DATA
+12V	A97	B97	NC
+12V	A98	B98	NC
+12V	A99	B99	NC
GND	A100	B100	GND
+12V	A101	B101	+12V
+12V	A102	B102	+12V
+12V	A103	B103	+12V
+12V	A104	B104	+12V
+12V	A105	B105	+12V
+12V	A106	B106	+12V
+12V	A107	B107	+12V
+12V	A108	B108	+12V
+12V	A109	B109	+12V
GND	A110	B110	GND

2.3.2 Signal Description – COM Express Connector 1 (CN2A)

2.3.2.1 Audio Signals

Signal	Signal Description
AC_SYNC	48kHz fixed-rate, sample-synchronization signal to the CODEC(s)
AC_RST#	Reset output to AC97 CODEC, active low.
AC_SDIN[0:2]	Serial TDM data inputs from up to 3 CODECs.
AC_BITCLK	12.228 MHz serial data clock generated by the external CODEC(s)
AC_SDOUT	Serial TDM data output to the CODEC.

2.3.2.2 Gigabit Ethernet Signals

Signal	Signal Description
GBE0_MD[0:3] +/-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:

	1000B-T	100B-T	10B-T
MDI[0]+/-	B1_DA+/	TX+/-	TX+/-
MDI[1]+/	B1_DB+/	RX+/-	RX+/-
MDI[2]+/	B1_DC+/	X	X
MDI[3]+/	B1_DD+/	X	X

GBE0_ACT#	Gigabit Ethernet Controller 0 activity indicator, active low.
GBE0_Link#	Gigabit Ethernet Controller 0 link indicator, active low.
GBE0_Link100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.
GBE0_Lin1000#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.

2.3.2.3 GPIO Signals

Signal	Signal Description
GPI[0:3]	General purpose input pins. Pulled high internally on the module.
GPO[0:3]	General purpose output pins. Upon a hardware reset, these outputs will be low.

2.3.2.4 Flat Panel LVDS Signals

Signal	Signal Description
BIASON	Controls panel contrast voltage.
DIGON	Controls panel digital power.
ENBKL#	Controls backlight power enable.
I^2C_DAT, I^2C_CLK	I^2C interface for panel parameter EEPROM. This EERPOM is mounted on the LVDS receiver. The data in the EEPROM allows the EXT module to automatically set the proper timing parameters for a specific LCD panel.

2.3.2.5 LPC Signals

Signal	Signal Description
LPC_FRAME#	LPC frame indicates the start of an LPC cycle
LPC_AD[0:3]	LPC multiplexed address, command and data bus
LPC_DRQ[0:1]#	LPC serial DMA request
LPC_CLK	LPC clock output - 33MHz nominal
LPC_SERIRQ	LPC serial interrupt

2.3.2.6 Miscellaneous Signals

Signal	Signal Description
I^2C_CK	General purpose I^2C port clock output
I^2C_DAT	General purpose I^2C port data I/O line
SPKR	Output for audio enunciator - the "speaker" in PC-AT systems
BIOS_DISABLE#	Module BIOS disable input. Pull low to disable module BIOS. Used to allow off-module BIOS implementations.
KB_RST#	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.
KB_A20GATE	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled low on the module.

2.3.2.7 PCI Express Signals

Signal	Signal Description
PCIE_TX[0:4] +/-	PCI Express Differential Transmit Pair 0-4
PCIE_RX[0:4] +/-	PCI Express Differential Receive Pair 0-4
PCIE0_CK_REF+/-	Reference clock output for PCI Express lanes 0-7 and for PCI Express Graphics lanes 0-15

2.3.2.8 Power Signals

Signal	Signal Description
VCC_5V_SBY	Standby power input: +5.0V nominal. See Electrical Specifications for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) must be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.
VCC_RTC	Real-time clock circuit-power input. Nominally +3.0V. See Electrical Specifications section for details.

2.3.2.9 Power & System Management Signals

Signal	Signal Description
SUS_S3#	Indicates system is in Suspend to RAM state. Active low output.
SUS_S4#	Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.
BATLOW#	Indicates that external battery is low
PWRBTN#	Power button to bring system out of S5 (soft off), active on rising edge.
SMB_CK	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.
SMB_DTA	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.
SMB_ALERT#	System Management Bus Alert - input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.
SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices
PWR_OK	Power OK from main power supply
THRMTRIP#	Active low output indicating that the CPU has entered thermal shutdown.
THRM#	Input from off-module temp sensor indicating and over-temp situation.
SYS_RESET#	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release.
RSMRST#	Resume reset input, active low. Resets power plane logic. May be left open on carrier board if not used.
WAKE0#	PCI Express wake up signal
WAKE1#	General purpose wake up signal

2.3.2.10 SATA Signals

Signal	Signal Description
SATA[0:3]_TX +/-	Serial ATA Channel 0-3 transmit differential pair.
SATA[0:3]_RX +/-	Serial ATA Channel 0-3receive differential pair.
ATA_ACT#	ATA (parallel and serial) activity indicator, active low.

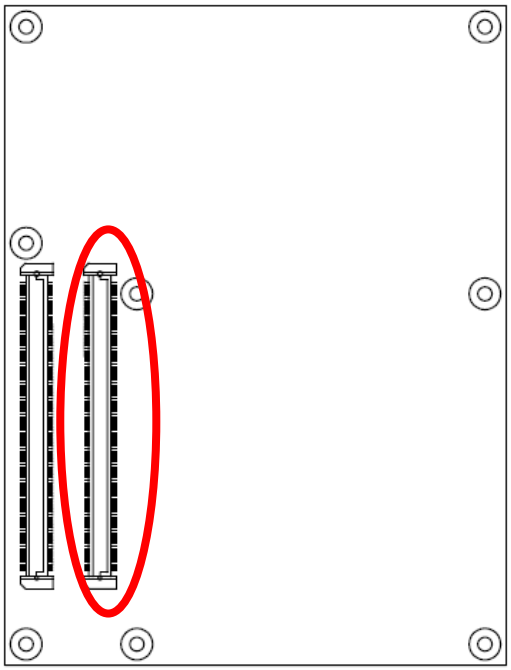
2.3.2.11 VGA Signals

Signal	Signal Description
VGA_RED	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.
VGA_GRN	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.
VGA_BLU	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.
VGA_HSYNC	Horizontal sync output to VGA monitor
VGA_VSYNC	Vertical sync output to VGA monitor
VGA_ I^2C_CK	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)
VGA_ I^2C_DAT	DDC data line.

2.3.2.12 USB Signals

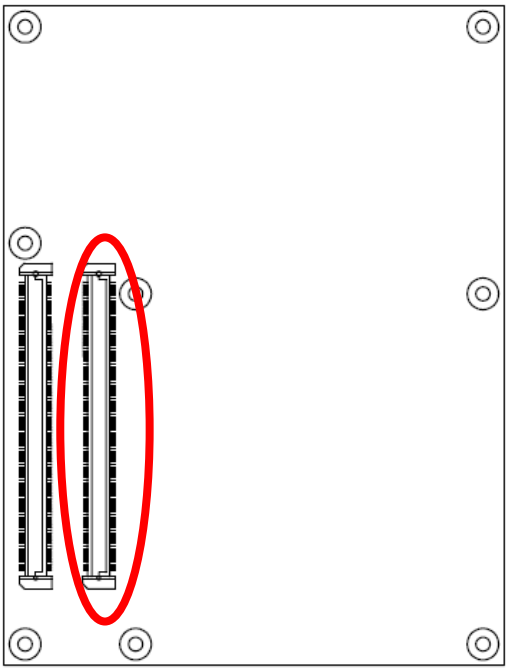
Signal	Signal Description
USB[0:7] +/-	USB differential pairs, channels 0 through 7
USB_0_1_OC#	USB over-current sense, USB channels 0 and 1
USB_2_3_OC#	USB over-current sense, USB channels 2 and 3
USB_4_5_OC#	USB over-current sense, USB channels 4 and 5
USB_6_7_OC#	USB over-current sense, USB channels 6 and 7

2.3.3 COM Express Connector 2 (CN2B)



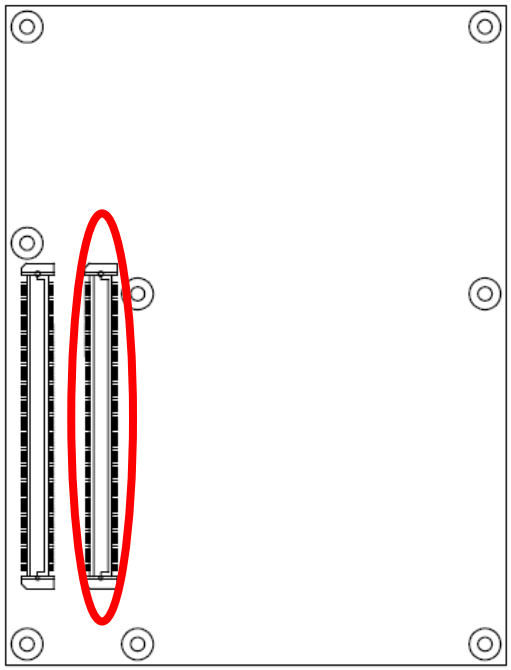
(Rear side)

Signal	PIN	PIN	Signal
GND	C1	D1	GND
IDE_PDD7	C2	D2	IDE_PDD5
IDE_PDD6	C3	D3	IDE_PDD10
IDE_PDD3	C4	D4	IDE_PDD11
IDE_PDD15	C5	D5	IDE_PDD12
IDE_PDD8	C6	D6	IDE_PDD4
IDE_PDD9	C7	D7	IDE_PDD0
IDE_PDD2	C8	D8	IDE_PDDREQ
IDE_PDD13	C9	D9	IDE_PDIOW#
IDE_PDD1	C10	D10	IDE_PDDACK#
GND	C11	D11	GND
IDE_PDD14	C12	D12	IDE_IRQ
IDE_PDIORDY	C13	D13	IDE_PDA0
IDE_PDIOR#	C14	D14	IDE_PDA1
PCI_PME#	C15	D15	IDE_PDA2
PCI_GNT#2	C16	D16	IDE_PDCS1#
PCI_REQ#2	C17	D17	IDE_PDCS3#
PCI_GNT#1	C18	D18	BUF_PLTRST#
PCI_REQ#1	C19	D19	PCI_GNT#3
PCI_GNT#0	C20	D20	PCI_REQ#3
GND	C21	D21	GND
PCI_REQ#0	C22	D22	PCI_AD1
PCIRST#	C23	D23	PCI_AD3
PCI_AD0	C24	D24	PCI_AD5
PCI_AD2	C25	D25	PCI_AD7
PCI_AD4	C26	D26	PCI_CBE#0
PCI_AD6	C27	D27	PCI_AD9
PCI_AD8	C28	D28	PCI_AD11
PCI_AD10	C29	D29	PCI_AD13
PCI_AD12	C30	D30	PCI_AD15



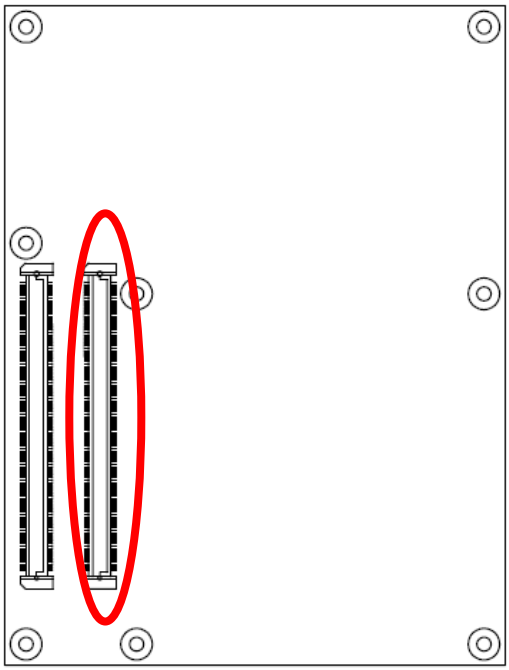
(Rear side)

Signal	PIN	PIN	Signal
GND	C31	D31	GND
PCI_AD14	C32	D32	PCI_PAR
PCI_CBE#1	C33	D33	PCI_SERR#
PCI_PERR#	C34	D34	PCI_STOP#
PCI_LOCK#	C35	D35	PCI_TRDY#
PCI_DEVSEL#	C36	D36	PCI_FRAME#
PCI_IRDY#	C37	D37	PCI_AD16
PCU_CBE#2	C38	D38	PCI_AD18
PCI_AD17	C39	D39	PCI_AD20
PCI_AD19	C40	D40	PCI_AD22
GND	C41	D41	GND
PCI_AD21	C42	D42	PCI_AD24
PCI_AD23	C43	D43	PCI_AD26
PCU_CBE#3	C44	D44	PCI_AD28
PCI_AD25	C45	D45	PCI_AD30
PCI_AD27	C46	D46	INT_PIRQC#
PCI_AD29	C47	D47	INT_PIRQD#
PCI_AD31	C48	D48	PM_CLKRUN#
INT_PIRQA#	C49	D49	NC
INT_PIRQB#	C50	D50	CLK_PCI
GND	C51	D51	GND
PEG_RX0	C52	D52	PEG_TX0
PEG_RX#0	C53	D53	PEG_TX#0
NC	C54	D54	PEG_LAN_RV#
PEG_RX1	C55	D55	PEG_TX1
PEG_RX#1	C56	D56	PEG_TX#1
NC	C57	D57	NC
PEG_RX2	C58	D58	PEG_TX2
PEG_RX#2	C59	D59	PEG_TX#2
GND	C60	D60	GND



(Rear side)

Signal	PIN	PIN	Signal
PEG_RX3	C61	D61	PEG_TX3
PEG_RX#3	C62	D62	PEG_TX#3
DDPB_AUX+	C63	D63	DDPC_AUX+
DDPB_AUX-	C64	D64	DDPC_AUX-
PEG_RX4	C65	D65	PEG_TX4
PEG_RX#4	C66	D66	PEG_TX#4
HDMIC_CTRL_CLK	C67	D67	GND
PEG_RX5	C68	D68	PEG_TX5
PEG_RX#5	C69	D69	PEG_TX#5
GND	C70	D70	GND
PEG_RX6	C71	D71	PEG_TX6
PEG_RX#6	C72	D72	PEG_TX#6
SDVO/HDMIB_CTRL_DATA	C73	D73	SDVO/HDMIB_CTRL_CLK
PEG_RX7	C74	D74	PEG_TX7
PEG_RX#7	C75	D75	PEG_TX#7
GND	C76	D76	GND
HDMIC_CTRL_DATA	C77	D77	PDIAG_S
PEG_RX8	C78	D78	PEG_TX8
PEG_RX#8	C79	D79	PEG_TX#8
GND	C80	D80	GND
PEG_RX9	C81	D81	PEG_TX9
PEG_RX#9	C82	D82	PEG_TX#9
HDMIB_HPD	C83	D83	NC
GND	C84	D84	GND
PEG_RX10	C85	D85	PEG_TX10
PEG_RX#10	C86	D86	PEG_TX#10
GND	C87	D87	GND
PEG_RX11	C88	D88	PEG_TX11
PEG_RX#11	C89	D89	PEG_TX#11
GND	C90	D90	GND



(Rear side)

Signal	PIN	PIN	Signal
PEG_RX12	C91	D91	PEG_TX12
PEG_RX#12	C92	D92	PEG_TX#12
GND	C93	D93	GND
PEG_RX13	C94	D94	PEG_TX13
PEG_RX#13	C95	D95	PEG_TX#13
GND	C96	D96	GND
HDMIC_HPD	C97	D97	NC
PEG_RX14	C98	D98	PEG_TX14
PEG_RX#14	C99	D99	PEG_TX#14
GND	C100	D100	GND
PEG_RX15	C101	D101	PEG_TX15
PEG_RX#15	C102	D102	PEG_TX#15
GND	C103	D103	GND
+12V	C104	D104	+12V
+12V	C105	D105	+12V
+12V	C106	D106	+12V
+12V	C107	D107	+12V
+12V	C108	D108	+12V
+12V	C109	D109	+12V
GND	C110	D110	GND

2.3.3 Signal Description – COM Express Connector 2 (CN2B)

2.3.3.1 IDE Signals

Signal	Signal Description
IDE_D[0:15]	Bidirectional data to / from IDE device.
IDE_A[0:2]	Address lines to IDE device.
IDE_REQ#	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.
IDE_IOW#	I/O write line to IDE device. Data latched on trailing (rising) edge.
IDE_ACK#	IDE Device DMA Acknowledge.
IDE_IRQ	Interrupt request from IDE device.
IDE_IORDY	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.
IDE_IOR#	I/O read line to IDE device.
IDE_CS1#	IDE Device Chip Select for 1F0h to 1FFh range.
IDE_CS3#	IDE Device Chip Select for 3F0h to 3FFhrange.
IDE_RESET#	Reset output to IDE device, active low.

2.3.3.2 HDMI Signals

Signal	Signal Description
SDVO/HDMIB_CTRL_DATA	SDVO or HDMI portB Control data
SDVO/HDMIB_CTRL_CLK	SDVO or HDMI portB Control clock
HDMIB_HPD	Reserved for HDMI portB hot plug detection (add a resistor on **R544** to activate)
HDMIC_CTRL_DATA	Reserved for HDMI portC Control data (add a resistor on **R180** to activate)
HDMIC_CTRL_CLK	Reserved for HDMI portC Control clock (add a resistor on **R188** to activate)
HDMIC_HPD	Reserved for HDMI portC hot plug detection (add a resistor on **R545** to activate)

2.3.3.3 PCI Signals

Signal	Signal Description
PCI_AD[0:31]	PCI bus multiplexed address and data lines
PCI_PME#	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.
PCI_GNT[0:3]#	PCI bus master grant output lines, active low.
PCI_REQ[0:3]#	PCI bus master request input lines, active low.
PCI_RESET#	PCI Reset output, active low.
PCI_CBE[0:3]	PCI bus byte enable lines, active low
PCI_PERR#	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.
PCI_LOCK#	PCI Lock control line, active low.
PCI_DEVSEL#	PCI bus Device Select, active low.
PCI_IRD Y#	PCI bus Initiator Ready control line, active low.
PCI_IRQ[A:D]	PCI interrupt request lines.
PCI_PAR	PCI bus parity
PCI_SERR#	System Error: SERR# can be pulsed active by any PCI device that detects a system error condition.
PCI_STOP#	PCI bus STOP control line, active low, driven by cycle initiator.
PCI_TRDY#	PCI bus Target Ready control line, active low.
PCI_FRAME#	PCI bus Frame control line, active low.
PCI_CLKRUN#	Bidirectional pin used to support PCI clock run protocol for mobile systems.
PCI_CLK	PCI 33MHz clock output.

2.3.3.4 PCI Express Graphics Signals

Signal	Signal Description
PEG_RX[0:15] +/-	PCI Express Graphics receive differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section).
PEG_TX[0:15] +/-	PCI Express Graphics transmit differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section).
TYPE[0:2]	
PEG_LANE_RV#	PCI Express Graphics lane reversal input strap. Pull low to reverse lane order. Pulled high on module.
SDVO_DATA	SDVO I^2C data line - to set up SDVO peripherals.
SDVO_CLK	SDVO I^2C clock line - to set up SDVO peripherals.