User's Manual

ECB-875/875L

Intel Pentium 4 Full-size PICMG CPU Card
with 533 MHz FSB, 4 USB 2.0, Audio, & Dual 10/100 Base-Tx Ethernet

1st Ed. – 7 November 2003

Part No.2047875000

FCC STATEMENT

THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE

RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

THESE LIMITS ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINTST HARMFUL INTERFERENCE WHEN THE EQUIPMENT IS OPERATED IN A COMMERCIAL ENVIRONMENT. THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTATLLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE HARMFUL INTERFERENCE TO RADIO COMMUNICATIONS.

OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE HARMFUL INTERFERENCE IN WHICH CASE THE USER WILL BE REQUIRED TO CORRECT THE INTERFERENCE AT HIS OWN EXPENSE.

Copyright Notice

Copyright © 2003 Evalue Technology Inc., ALL RIGHTS RESERVED.

No part of this document may be reproduced, copied, translated, or transmitted in any form or by any means, electronic or mechanical, for any purpose, without the prior written permission of the original manufacturer.

Trademark Acknowledgement

Brand and product names are trademarks or registered trademarks of their respective owners.

Disclaimer

Evalue Technology Inc. reserves the right to make changes, without notice, to any product, including circuits and/or software described or contained in this manual in order to improve design and/or performance. Evalue Technology assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright, or masks work rights to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described in this manual are for illustration purposes only. Evalue Technology Inc. makes no representation or warranty that such application will be suitable for the specified use without further testing or modification.

Life Support Policy

Evalue Technology's PRODUCTS ARE NOT FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE PRIOR WRITTEN APPROVAL OF Evalue Technology Inc.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labelling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

A Message to the Customer

Evalue Customer Services

Each and every Evalue's product is built to the most exacting specifications to ensure reliable performance in the harsh and demanding conditions typical of industrial environments. Whether your new Evalue device is destined for the laboratory or the factory floor, you can be assured that your product will provide the reliability and ease of operation for which the name Evalue has come to be known.

Your satisfaction is our primary concern. Here is a guide to Evalue's customer services. To ensure you get the full benefit of our services, please follow the instructions below carefully.

Technical Support

We want you to get the maximum performance from your products. So if you run into technical difficulties, we are here to help. For the most frequently asked questions, you can easily find answers in your product documentation. These answers are normally a lot more detailed than the ones we can give over the phone. So please consult this manual first.

To receive the latest version of the user manual, please visit our Web site at:

http://www.evalue-tech.com/

If you still cannot find the answer, gather all the information or questions that apply to your problem, and with the product close at hand, call your dealer. Our dealers are well trained and ready to give you the support you need to get the most from your Evalue's products. In fact, most problems reported are minor and are able to be easily solved over the phone.

In addition, free technical support is available from Evalue's engineers every business day. We are always ready to give advice on application requirements or specific information on the installation and operation of any of our products. Please do not hesitate to call or e-mail us.

Headquarters
Evalue Technology Inc.
5F~7, No.130, Chien Kang Road,
Chung Ho City, Taipei,
Taiwan
Tel : +886-2-2228-6111
Fax : +886-2-2228-6667
http://www.evalue-tech.com
E-mail: service@evalue-tech.com

Europe Branch Office
Evalue Europe A/S
Nordre Strandvej 119C,
3150 Hellebaek,
Denmark
Tel : +45-7025-0310
Fax : +45-4975-5026
http://www.evalue-tech.com
E-mail: service.europe@evalue-tech.com

China Branch Office
Evalue Technology Shanghai Inc.
Room 909, 9F, Section B, No.900,
Yisan Road, Caohejing Hi-tech Park,
Shanghai 200233, China
Tel : +86-21-5423-4170
Fax : +86-21-5423-4171
http://www.evalue-tech.com
E-mail: service.china@evalue-tech.com

Product Warranty

Evalue warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Evalue, or which have been subject to misuse, abuse, accident or improper installation. Evalue assumes no liability under the terms of this warranty as a consequence of such events. Because of Evalue's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If any of Evalue's products is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details. If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU type and speed, Evalue's products model name, hardware & BIOS revision number, other hardware and software used, etc.) Note anything abnormal and list any on-screen messages you get when the problem occurs.

2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information available.

3. If your product is diagnosed as defective, obtain an RMA (return material authorization) number from your dealer. This allows us to process your good return more quickly.

4. Carefully pack the defective product, a complete Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.

5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 ECB-875 Pentium 4 Full-size CPU card
- 1 Quick Installation Guide
- 1 CD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Latest BIOS (as of the CD-ROM was made)
- Cable set includes the followings:
  - 1 ATA-100 IDE cable (40-pin, pitch 2.54mm)
  - 1 FDD cable (34-pin, pitch 2.54mm)
  - 1 bracket with one printer and one serial port (10-pin, 2.54mm/26-pin, pitch 2.54mm)
  - 1 PS/2 keyboard and mouse Y cable (6-pin, Mini-DIN)

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

1. MANUAL OBJECTIVES 1

2. INTRODUCTION 2

2.1 System Overview 2

2.2 System Specifications 3

2.3 Architecture Overview 5
2.3.1 82845GV MCH and 82801DB 6
2.3.2 System Memory Controller 6
2.3.3 Multiplexed Intel DVO Port Interface 7
2.3.4 PCI Interface 7
2.3.5 IDE Interface (Bus Master Capability and Synchronous DMA Mode) 7
2.3.6 Low Pin Count (LPC) Interface 7
2.3.7 USB 2.0 8
2.3.8 Ethernet 8
2.3.9 M-Systems DiskOnChip 9

3. HARDWARE CONFIGURATION 10

3.1 Installation Procedure 10

3.2 Safety Precautions 10
3.2.1 Warning! 10
3.2.2 Caution! 10

3.3 Socket 478 Processor 11
3.3.1 Installing Pentium 4 CPU 11
3.3.2 Removing CPU 11

3.4 Main Memory 11

3.5 M-Systems' DiskOnChip Flash Disk 12
3.5.1 Installing DOC 12

3.6 Installing the Single Board Computer 12
3.6.1 Drivers Support 13

3.7 Jumper & Connector 14
3.7.1 Jumper & Connector Layout 14
3.7.2 Jumper & Connector List 15

3.8 Setting Jumpers 17
3.8.1 External Speaker Select (J3) 18
3.8.2 COM2 RS-232/422/485 Select (J4, J6) 18
3.8.3 COM1 / 2 Pin 9 Signal Select (J7, J8) 19
3.8.4 Compact Flash Mode Select (J9) 20
3.8.5 CPU FSB Frequency Select (J11) 20
3.8.6 Clear CMOS (J12) 20
3.8.7 M-Systems DiskOnChip Memory Address Select (J13) 20

3.9 Connector Definitions 21
3.9.1 CD-ROM Audio Input Connector (CD_IN1) 21
3.9.2 Signal Description – CD-ROM Audio Input Connector (CD_IN1) 21
3.9.3 Pentium IV +12V Connector (CN1) 21
3.9.4 External SM Bus Connector (CN2) 21
3.9.5 Power Fan Connector (CN3) 21
3.9.6 Signal Description – Power Fan Connector (CN3) 21
3.9.7 CPU Fan Connector (CN4) 22
3.9.8 Signal Description – CPU Fan Connector (CN4) 22
3.9.9 Front Panel Connector (CN5) 22
3.9.10 External Standby Power Connector (CN6) 22
3.9.11 Primary IDE Connector (CN7) 23
3.9.12 Secondary IDE Connector (CN8) 24
3.9.13 Signal Description – Primary & Secondary and RAID IDE Connector (CN7, CN8) ... 25
3.9.14 Floppy Connector (CN9) 28
3.9.15 Signal Description – Floppy Connector (CN9) 29
3.9.16 Parallel Port Connector (CN10) 29
3.9.17 Signal Description – Parallel Port Connector (CN10) 30
3.9.18 Serial Port 2 Connector (CN11) 30
3.9.19 Serial Port 2 with External DB9 Connector (CN11) 31
3.9.20 Signal Description – Serial Port 1 / 2 Connector (CN16, CN11) 31
3.9.21 DVO Port B (CN12) 32
3.9.22 DVO Port C (CN13) 33
3.9.23 Signal Description – DVO port B & DVO port C (CN12, CN13) 34
3.9.24 Audio Output Connector (CN14) 36
3.9.25 Daughter Board Connector A (CN15) 36
3.9.26 Daughter Board Connector B (CN21) 36
3.9.27 IrDA Connector (CN17) 37
3.9.28 Signal Configuration –IrDA Connector (CN17) 37
3.9.29 10/100 BASE-Tx Ethernet Connector (CN19) 37
3.9.30 Signal Description – 10/100Base-Tx Ethernet Connector (CN19) 37
3.9.31 USB Connector (CN20) 37
3.9.32 Signal Description – USB Connector (CN20) 38
3.9.33 VGA Connector (CN22) 38
3.9.34 Signal Description – VGA Connector (CN22) 38
3.9.35 Power Connector (CN23) 39
3.9.36 Chassis Fan Connector (CN24) 39
3.9.37 Signal Description – Chassis Fan Connector 39
3.9.38 North Bridge Fan Connector (CN25) 39
3.9.39 Internal Keyboard Connector (CN26) 39
3.9.40 Signal Description – Internal Keyboard Connector (CN26) 39
3.9.41 PS/2 Keyboard & Mouse Connector (CN27) 40
3.9.42 Signal Description – PS/2 Keyboard & Mouse Connector (CN27) 40
3.9.43 Auxiliary Power Connector (J2) 40

4. AWARD BIOS SETUP 41

4.1 Starting Setup 41

4.2 Using Setup 42
4.2.1 Navigating through the menu bar 42
4.2.2 To display a sub menu 42

4.3 Getting Help 43

4.4 In Case of Problems 43

4.5 Main Menu 43
4.5.1 Setup Items 44
4.5.2 Standard CMOS Setup 45
4.5.3 Advanced CMOS Setup Defaults 48
4.5.4 Advanced Chipset Setup Defaults 51
4.5.5 Integrated Peripherals Setup Defaults 54
4.5.6 Power Management Setup Defaults 58
4.5.7 PnP/ PCI Setup Defaults 62
4.5.8 PC Health Status Setup Defaults 64
4.5.9 Current CPUFAN , CHASFAN & PWRFAN Speed 64
4.5.10 Load Fail-Safe Defaults 67
4.5.11 Load Optimized Defaults 67
4.5.12 Set Supervisor/User Password 68
4.5.13 Save & Exit Setup 68
4.5.14 Exit Without Saving 68

4.6 Flash BIOS Utility 68

5. DRIVER INSTALLATION 69

5.1 Driver Installation for Ethernet Adapter 69
5.1.1 Windows 9x 69
5.1.2 Windows 2000 Ethernet Installation 74

5.2 Driver Installation for Display Adapter 81
5.2.1 Windows 9x 81
5.2.2 Windows 2000 or Windows XP Display Installation 84

5.3 Driver Installation for Audio Adapter 87
5.3.1 Windows 9x, Windows 2000, Windows XP 87

5.4 Driver Installation for Intel 845 Chipset 89

5.5 Driver Installation for Intel 845G USB2.0 92
5.5.1 Windows 9x 92
5.5.2 Windows 2000 USB 2.0 Installation 94

6. MEASUREMENT DRAWING 100

APPENDIX A: BIOS REVISIONS 101

APPENDIX B: SYSTEM RESOURCES 102
Memory Map 102
I/O – Map 103
Interrupt Usage. 105
DMA-channel Usage 106

APPENDIX C: AWARD BIOS POST MESSAGES 107

POST Beep 107

Error Messages 107
CMOS Battery Has Failed 107
CMOS Checksum Error 107
Disk Boot Failure, Insert System Disk And Press Enter 107
Diskette Drives Or Types Mismatch Error – Run Setup 107
Display Switch Is Set Incorrectly 107
Display Type Has Changed Since Last Boot 108
EISA Configuration Checksum Error Please Run EISA Configuration Utility 108
EISA Configuration Is Not Complete Please Run EISA Configuration Utility 108
Error Encountered initializing Hard Drive 108
Error Initializing Hard Disk Controller 108
Floppy Disk Cntrlr Error Or No Cntrlr Present 108
Invalid EISA Configuration Please Run EISA Configuration Utility 108
Keyboard Error Or No Keyboard Present 109
Memory Address Error At... 109
Memory Parity Error At... 109
Memory Size Has Changed Since Last Boot 109
Memory Verify Error At... 109
Offending Address Not Found 109
Offending Segment 109
Press A Key To Reboot 109
Press F1 To Disable NMI, F2 To Reboot 109
RAM Parity Error – Checking For Segment 110
Should Be Empty But EISA Board Found Please Run EISA Configuration Utility 110
Should Have EISA Board But Not Found Please Run EISA Configuration Utility 110
Slot Not Empty 110
System Halted, (CTRL-ALT-DEL) To Reboot 110
Wrong Board In Slot Please Run EISA Configuration Utility 110
Floppy Disk(s) Fail (80) → Unable To Reset Floppy Subsystem. 110
Floppy Disk(s) Fail (40) → Floppy Type Dismatch. 110
Hard Disk(s) Fail (80) → HDD Reset Failed 110
Hard Disk(s) Fail (40) → HDD Controller Diagnostics Failed. 110
Hard Disk(s) Fail (20) → HDD Initialization Error. 110
Hard Disk(s) Fail (10) → Unable To Recalibrate Fixed Disk. 111
Hard Disk(s) Fail (08) → Sector Verify Failed. 111
Keyboard Is Locked Out - Unlock The Key. 111
Keyboard Error Or No Keyboard Present. 111
Manufacturing POST Loop. 111
BIOS ROM Checksum Error - System Halted. 111

Memory Test Fail. 111

APPENDIX D: AWARD BIOS POST CODES..... 112

Document Amendment History

Revision	Date	By	Comment
1st	November. 2003	Stephen Tsao	Initial Release

1. Manual Objectives

This manual describes in detail the Evalue Technology ECB-875 Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board. The manual is sectioned and includes a User's Guide that will help the non-technical user to get the unit up and running. A Troubleshooting Guide is also included to help when things go wrong.

We strongly recommend that you study this manual carefully before attempting to interface with ECB-875 or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

2. Introduction

2.1 System Overview

The ECB-875 is an all-in-one Full-size Pentium 4 Single Board Computer (SBC) designed with Intel embedded chipset 845GV which supports the latest Intel m-PGA 478 Pentium 4 CPU with FSB up to 533 MHz, dual PCI-bus Fast Ethernet controllers, and M-Systems DiskOnChip socket.

Targeting on the mission critical telecommunication or industrial applications, the ECB-875 comes designed with Intel 82845GV Chipset - Intel EMD solutions. Unlike regular commercial solutions, Intel EMD solutions provide higher system stability and longer product supply time (Intel EMD products' typical life cycle is 5 years). The long product life cycle guarantee is particularly important for systems that are designed to last for many years. This makes it a perfect solution for not only popular Networking Devices like Firewall, Gateway, Router, and e-Server, but also CTI (Computer Telephony Integration) equipments such as PBX, Digital Logger, etc.

Other onboard features include 533 MHz FSB, four UDMA 100 IDE channels, two 16C550 compatible serial ports (one RS-232, one RS-232/422/485), one multi-mode parallel port, and two 184-pin DIMM sockets allowing for up to 2GB of DDR SDRAM to be installed.

2.2 System Specifications

General Functions

- **CPU:** Intel Pentium 4 CPU with FSB up to 533 MHz
- **CPU Socket:** Intel Socket 478
- **BIOS:** Award 4Mbit Flash BIOS
- **Chipset:** Intel 82845GV GMCH + 82801DB ICH4
- **I/O Chipset:** Winbond W83627HF
- **Memory:** Onboard two DDR SDRAM socket supports up to 2 Gbytes DDR 266/200 SDRAM
- **Watchdog Timer:** Can generate a system reset, IRQ15 or NMI. Software selectable time out interval (2 sec. ~ 255 sec., 1 sec./step)

I/O Interface

- **Multi I/O:** EIDE x 2 (UDMA 100), FDD x 1, K/B x 1, Mouse x 1, RS-232 x 1, RS-232/422/485 x 1, LPT x 1
- **IrDA:** 115kbps, IrDA 1.0 compliant
- **USB:** USB port x 2, USB 2.0 compliant (5 x 2 header)
- **SSD:** One 32-pin DIP socket supports M-Systems DiskOnChip 2000 series up to 1 GBytes

Ethernet Interface

- **Chipset:** Dual Realtek 8100B or Intel 82550/82559/82559ER PCI-bus Ethernet controllers onboard
- **Ethernet Interface:** PCI 100/10 Mbps, IEEE 802.3U compatible

Video Interface

- **Chipset:** Intel 82845GV GMCH AGP 4X high performance 256-bit GUI VGA controller with 3D/2D engine
- **Memory:** 4/8 MB frame buffer using system memory

Resolution: Display mode:

LCD panel supports up to 2048 x 1536 @ 60Hz

CRT displays support up to 2048 x 1536 @ 60Hz

SSD Interface

One 32-pin DIP socket supports M-Systems DiskOnChip 2000 series up to 1 GBytes

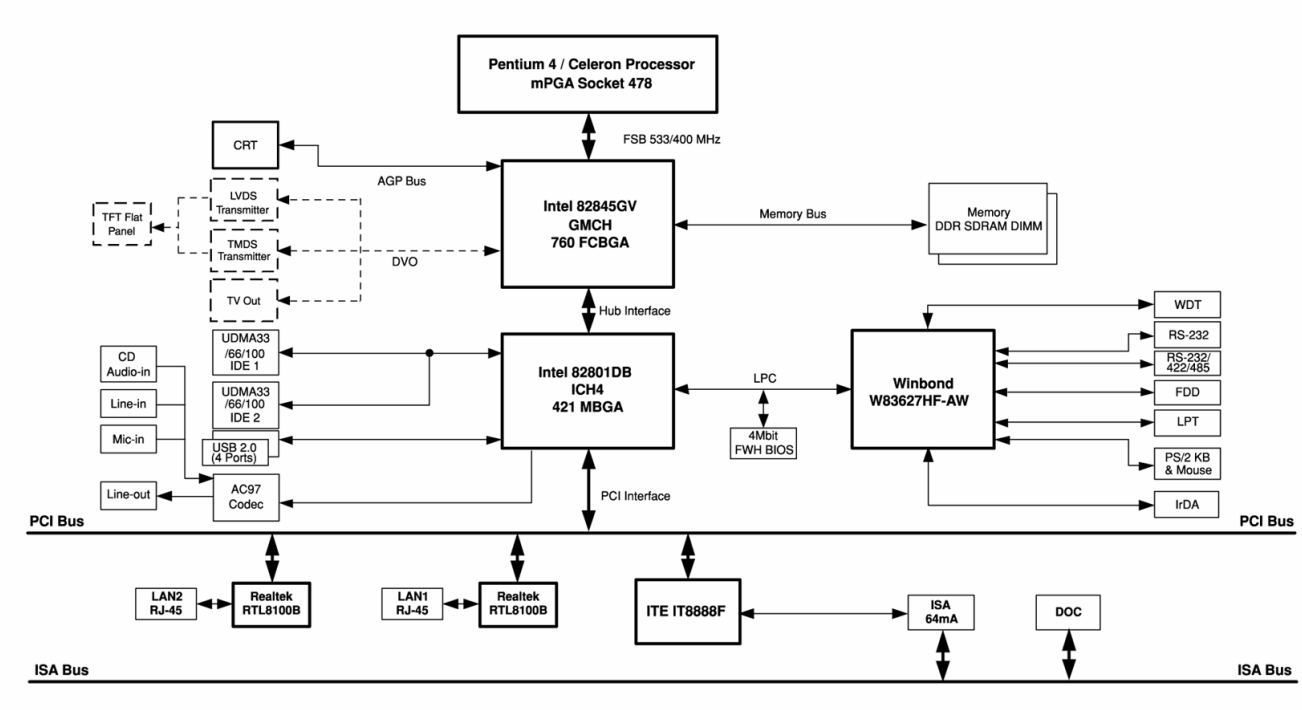
Compact Flash: One CF socket supports Type I / II Compact Flash Card

Mechanical and Environmental

- **Power Supply Voltage:** ATX type, +5V and +12V
- **Operating Temperature:** 0 to 60° C (32 to 140° F)
- **Board Size:** 13.3"(L) x 4.8"(W) (338 mm x 122 mm)
- **Weight:** 0.5 Kg

2.3 Architecture Overview

The following block diagram shows the architecture and main components of ECB-875. Two major chipsets on board are the 82845GV Graphic Memory Control Hub and 82801DB ICH4. These two devices provide interface to Socket478 processor, supports DDR SDRAM, PCI bus interface, ACPI compliant power management, USB 2.0 port, and Ultra DMA/33/66/100 IDE Bus Master. The 82801DB ICH4 also supports the standard I/O functions like PS/2 Keyboard/Mouse, two 16C550 UARTs, FDC, Parallel and Infrared interface. In addition, the onboard dual Realtek 8100B or Intel 82559ER 10/100BASE-TX Ethernet controller delivers high speed data transfers over the PCI bus.



The following sections provide detail information about the functions provided onboard.

2.3.1 82845GV MCH and 82801DB

The Intel® 845GV chipset support Pentium 4 processor with 256KB L2 cache and Pentium 4 processor with 512 KB L2 cache on 0.13 micro process. The processor interface supports the Pentium 4 processor subset of the Extended Mode of the Scalable Bus Protocol. In an 845GV chipset-based platform, I/O functions are integrated onto the ICH4.

The chipset platform supports either the integrated graphics device (IGD) on the GMCH or an external graphics device on AGP. The IGD has 3D, 2D, and video capabilities. The IGD also has two multiplexed Intel DVO ports to support DVO devices.

The ICH4 is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of functions needed in today's PC platform. The GMCH and ICH4 communicate over a dedicated hub interface. The 82801DB ICH4 functions and capabilities include:

- PCI Rev. 2.2 compliant with support for 33MHz PCI operations
- Supports up to 6 Request/Grant pairs (PCI slots)
- Power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated IDE controller; Ultra ATA/100/66/33
- USB host interface; 3 host controllers and supports 6 USB ports; includes a EHCI high-speed 2.0 USB controller
- Integrated LAN controller
- System Management Bus (SMBus) compatible with most IC devices; ICH4 has both bus master and slave capability
- AC '97 2.3 compliant link for audio and telephony codecs; up to 6 channels
- Low Pin Count (LPC) interface
- FWH Interface (FWH Flash BIOS support)
- Alert on LAN* (AOL and AOL2)

2.3.2 System Memory Controller

The GMCH can support DDR 266 and DD R200 in DDR mode with SSTL_2 signaling. The GMCH includes support for:

- *Up to 2 GB of 266 MHz or 200 MHz DDR SDRAM*
- *DDR266 or 200 unbuffered 184-pin non-ECC DDR SDRAM DIMMs*
- *Maximum of 2 DIMMs, single-sided and/or double-sided*

- *Byte masking on writes through data masking*

The bank address lines and the address lines allow the GMCH to support 64-bit wide DIMMs using 64-MBb 128-Mb, 256-Mb, and 512-Mb SDRAM technology. The four chip select lines support up to rows of double-side SDRAM DIMMs. For write operations of less than a Qword, the GMCH performs a byte-wise write. The GMCH does not support ECC DIMMs, registered DIMMs, or double-side x16 DIMMs.

2.3.3 Multiplexed Intel DVO Port Interface

The GMCH supports two multiplexed DVO ports that can each drive pixel clocks up to 165MHz.

2.3.4 PCI Interface

The ICH4 PCI interface provides a 33 MHz, Rev. 2.2 compliant implementation. All PCI signals are 5V tolerant, except PME#. The ICH2 integrates a PCI arbiter that supports up to six external PCI bus masters in addition to the internal ICH4 requests.

2.3.5 IDE Interface (Bus Master Capability and Synchronous DMA Mode)

The fast IDE interface supports up to four IDE devices providing an interface for IDE hard disks and ATAPI devices. Each IDE device can have independent timings. The IDE interface supports PIO IDE transfers up to 16 Mbytes/sec and Ultra ATA transfers up 100 Mbytes/sec. It does not consume any ISA DMA resources. The IDE interface integrates 16x32-bit buffers for optimal transfers.

The ICH4's IDE system contains two independent IDE signal channels. They can be electrically isolated independently. They can be configured to the standard primary and secondary channels (four devices). There are integrated series resistors on the data and control lines.

Access to these controllers is provided by two standard IDC 40-pin connectors.

2.3.6 Low Pin Count (LPC) Interface

The ICH4 implements an LPC Interface as described in the LPC 1.0 specification. The Low Pin Count (LPC) Bridge function of the ICH4 resides in PCI Device 31: Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, Interrupt controllers, Timers, Power Management, System Management, GPIO, and RTC.

Not that in the current chipset platform, the Super I/O (SIO) component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost Super I/O designs.

2.3.7 USB 2.0

The ICH4 contains an Enhanced Host Controller Interface (EHCI) compliant host controller that supports USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480Mb/s which is 40 times faster than full-speed USB. The ICH4 also contains three Universal Host Controller Interface (UHCI) controllers that support USB full-speed and low-speed signaling.

The ICH4 supports 6 USB 2.0 ports. All six USB ports are high-speed, full-speed, and low-speed capable. ICH4's port-routing logic determines whether a USB port is controlled by one of the UHCI controllers or by the EHCI controller.

2.3.8 Ethernet

2.3.8.1 ICH4 LAN Controller

ICH4's integrated LAN Controller includes a 32-bit PCI controller that provides enhanced scatter-gather bus mastering capabilities and enables the LAN Controller to perform high-speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high level commands and perform multiple operations, this lowers processor utilization by off-loading communication tasks from the processor. Two large transmit and receive FIFOs of 3 KB each help prevent data under runs and overruns while waiting for bus accesses. This enables the integrated LAN Controller to transmit data with minimum interframe spacing (IFS).

The LAN Controller can operate in either full duplex or half duplex mode. In full duplex mode the LAN Controller adheres with the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

The integrated LAN controller also includes an interface to a serial (4-pin) EEPROM. The EEPROM provides power-on initialization for hardware and software and software configuration parameters.

From a software perspective, the integrated LAN controller appears to reside on the secondary side of the ICH4's virtual PCI to PCI Bridge. This is typically Bus 1, but may be assigned a different number, depending on system configuration.

The following summarizes the ICH4 LAN controller features:

- *Compliance with Advanced Configuration and Power Interface and PCI Power Management standard.*
- *Support for wake-up on interesting packets and link status change*
- *Support for remote power-up using Wake on LAN (WOL) technology*
- *Deep power-down node support*
- *Support of Wired for management (WfM) Rev 2.0*
- *Backward compatible software with 82447, 82558 and 82559*
- *TCP/UDP checksum of f load capabilities*

- *Support for Intel's Adaptive Technology*

2.3.8.2 Realtek RTL8100B Ethernet Controller

The Realtek RTL8100B is one of the Realtek RTL8139A/B/C/8130 family, the highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that is capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management.

2.3.8.3 Intel 82559

The Ethernet interface is based on an Intel 82559 Ethernet controller that supports both 10BASE-T and 100BASE-TX. The 82559 consists of both the Media Access Controller (MAC) and the physical layer (PHY) interface combined into a single component solution.

The 32-bit PCI controller provides enhanced scatter-gather bus mastering capabilities and enables the 82559 to perform high speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers CPU utilization by off-loading communication tasks from the CPU. Two large transmit and receive FIFOs of 3 Kbytes each help prevent data under runs and overruns while waiting for bus accesses. This enables the 82559 to transmit data with minimum interframe spacing (IFS).

2.3.9 M-Systems DiskOnChip

M-Systems' DiskOnChip 2000 is a high performance single-chip flash disk in a standard 32-pin DIP package. This unique data storage solution offers cost effective data storage beyond that of traditional hard disks. Perfect for applications with limited space and varying capacity requirements. The DiskOnChip 2000 is simply inserted into a 32-pin DIP socket on your platform board and you have a bootable flash disk.

-
- Supports L1/L2 write-back forward to PCI master read to minimize PCI read latency
- Supports L1/L2 write-back merged with PCI master post-write to minimize DRAM utilization
- Delay transaction from PCI master reading DRAM
- Read caching for PCI master reading DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance

3. Hardware Configuration

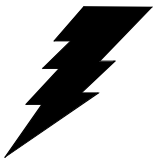
This chapter explains you the instructions of how to set up your system. The additional information shows you how to install M-Systems' DiskOnChip and program the Watchdog Timer.

3.1 Installation Procedure

1. Turn off the power supply.
2. Insert the DIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the PWR1.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the "Auto Configuration with Optimal Settings" feature. The ***Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilised, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

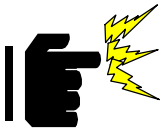
3.2 Safety Precautions

3.2.1 Warning!



Always completely disconnect the power cord from your chassis or power cable from your board whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

3.2.2 Caution!



Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

3.3 Socket 478 Processor

3.3.1 Installing Pentium 4 CPU

- Lift the handling lever of CPU socket outwards and upwards to the other end.
- Align the processor pins with pin holes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place. If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.
- Push down the lever to lock processor chip into the socket.
- Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the socket 478.
- Be sure to follow particular CPU speed and voltage type to adjust the jumper settings properly.

3.3.2 Removing CPU

- Unlock the cooling fan first.
- Lift the lever of CPU socket outwards and upwards to the other end.
- Carefully lift up the existing CPU to remove it from the socket.
- Follow the steps of installing a CPU to change to another one or place handling bar to close the opened socket.

3.4 Main Memory

ECB-875 provides 2 DIMM sockets (184-pin Dual In-line Memory Module) to support 1.5V DDR SDRAM. The maximum memory size is 2GB. Both single and double-side DIMM module can be used on ECB-870. And, it is not necessary to install the DIMM module in order. You can install different size of DDR SDRAM module on DIMM1, DIMM2, or both.

Watch out the contact and lock integrity of memory module with socket, it will influence the system's reliability. Follow the normal procedure to install your DDR SDRAM module into the DIMM socket. Before locking the DIMM module, make sure that the memory module has been completely inserted into the DIMM socket.

Note:

Please do not change any DDR SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.

3.5 M-Systems' DiskOnChip Flash Disk

ECB-875 reserves a 32-pin DIP socket to support M-Systems' DiskOnChip flash disk up to 1 GB. The DiskOnChip is based on pure ISA bus and without PnP (Plug and Play) function. Before the installation, make sure that the DiskOnChip I/O address jumper is set properly to prevent the I/O resource conflict.

3.5.1 Installing DOC

Align the DOC with the pinholes on the socket. Make sure that the notched corner or dot mark (pin 1) of DOC corresponds to notched corner of the socket. Then press the DOC gently until it fits into place. If installation procedure is correct, the flash disk can be viewed as a normal hard disk to access read/write data now.

Note:

> Please make sure that your DOC is properly inserted. Place the DOC in wrong direction will damage the flash device.

If you system would like to boot from the flash disk, it is recommended to refer to the application note provided by M-Systems first. You can easily obtain the application note from M-Systems' DiskOnChip user's manual or from their web site as below.

http://www.m-sys.com

3.6 Installing the Single Board Computer

To install your ECB-875 into chassis or proprietary environment, the following steps have to be followed.

- Make sure all jumpers are properly set.
- Install and configure CPU and memory module correctly.
- Place the ECB-875 into the dedicated position in your system.
- Attach cables to peripherals.

Note:

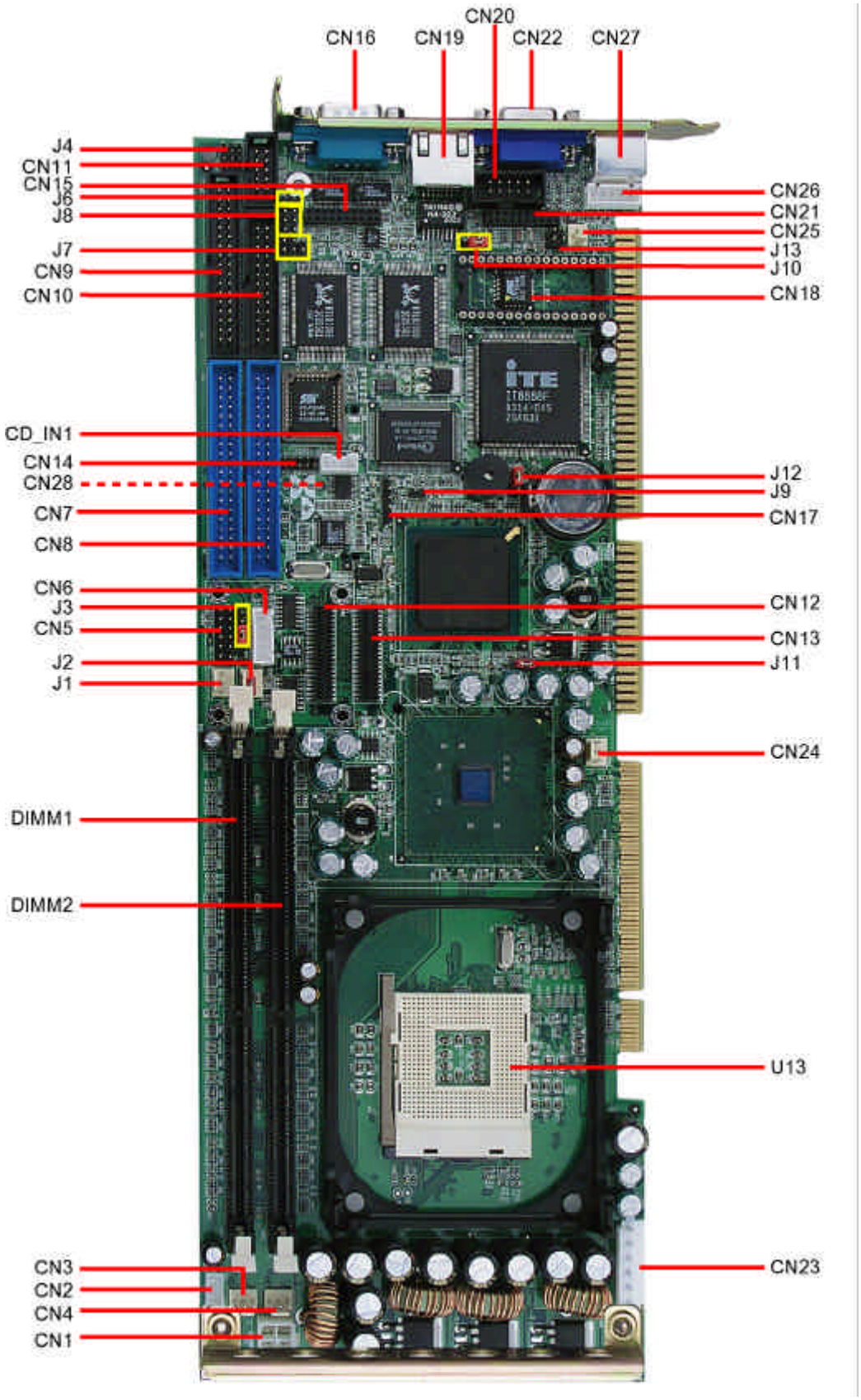
> Please ensure that your SBC is properly installed and fixed by mechanism. Otherwise, the system might be unstable or do not work due to bad contact of golden finger and slot.

3.6.1 Drivers Support

ECB-875 provides on CD-Title to support on-board VGA and Ethernet device drivers in various operating systems. Before installing the device drivers, please see the reference files in each sub-directory. You cannot install drivers from CD-Title directly.

3.7 Jumper & Connector

3.7.1 Jumper & Connector Layout



3.7.2 Jumper & Connector List

Connectors on the board are linked to external devices such as hard disk drives, keyboard, mouse, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

The following tables list the function of each of the board's jumpers and connectors.

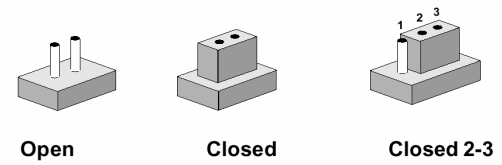
Jumpers		
Label	**Function**	**Note**
J3	External speaker select	4 x 1 header, pitch 2.54mm
J4, J6	COM2 RS-232/422/485 select	4 x 3 header, pitch 2.0mm (J4) 3 x 2 header, pitch 2.0mm
J5	Reserve for future use	3 x 1 header, pitch 2.54mm
J7	COM1 pin 9 signal select	3 x 2 header, pitch 2.54mm
J8	COM2 pin 9 signal select	3 x 2 header, pitch 2.54mm
J9	Compact Flash mode select	2 x 1 header, pitch 2.54mm
J10	Reserve for internal test only	3 x 1 header, pitch 2.54mm
J11	CPU FSB frequency select	3 x 1 header, pitch 2.54mm
J12	Clear CMOS	3 x 1 header, pitch 2.54mm
J13	M-Systems DiskOnChip memory address select	2 x 2 header, pitch 2.0mm

Connectors		
Label	**Function**	**Note**
CD_IN1	CD-ROM audio input connector	4 x 1 wafer, pitch 2.0mm
CN1	Pentium IV +12V connector	
CN2	External SM bus connector	4 x 1 wafer, pitch 2.0mm
CN3	Power fan connector	3 x 1 wafer, pitch 2.54mm
CN4	CPU fan connector	3 x 1 wafer, pitch 2.54mm
CN5	Front panel connector	6 x 2 header, pitch 2.54mm
CN6	External standby power connector	5 x 1 wafer, pitch 2.0mm
CN7	Primary IDE connector	20 x 2 box header, pitch 2.54mm
CN8	Secondary IDE connector	20 x 2 box header, pitch 2.54mm
CN9	Floppy connector	17 x 2 box header, pitch 2.54mm
CN10	Parallel port connector	13 x 2 box header, pitch 2.54mm
CN11	Serial port 2 connector	5 x 2 box header, pitch 2.54mm
CN12	DVO port B connector	Samtec CLM-120-02-L-D
CN13	DVO port C connector	Samtec CLM-120-02-L-D
CN14	Audio output connector	5 x 2 header, pitch 2.0mm
CN15	Daughter board connector A	
CN16	Serial port 1 connector	D-sub 9-pin male connector
CN17	IrDA connector	5 x 1 header, pitch 2.54mm
CN18	M-Systems DOC 2000 socket	16 x 2 DIP socket
CN19	10/100 Base-Tx Ethernet connector	RJ-45
CN20	USB connector	5 x 2 box header, pitch 2.54mm
CN21	Daughter board connector B	
CN22	VGA connector	D-sub 15-pin female connector
CN23	Power connector	
CN24	Chassis fan connector	3 x 1 wafer, pitch 2.54mm
CN25	North Bridge fan connector	2 x 1 wafer, pitch 2.54mm
CN26	Internal keyboard connector	5 x 1 wafer, pitch 2.54mm
CN27	PS/2 keyboard & mouse connector	6-pin mini DIN
CN28	Compact Flash connector	
DIMM 1, 2	184-pin DDR SDRAM DIMM socket	
J1	Reserved for future used	
J2	Auxiliary power connector	3 x 1 wafer, pitch 2.0mm

3.8 Setting Jumpers

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



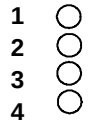
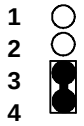
The jumper settings are schematically depicted in this manual as follows:

A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

3.8.1 External Speaker Select (J3)

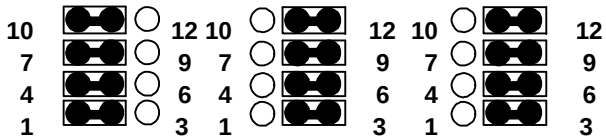
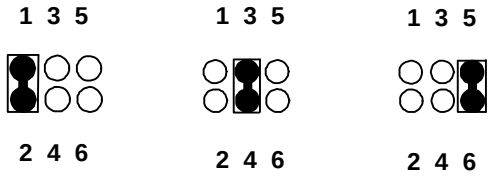
J3 is a 4-pin connector for an external speaker. If there is no external speaker, the ECB-875 provides an onboard buzzer as an alternative. To enable the buzzer, set pin 3-4 as closed.

External Speaker Select (J3)		
	External speaker	Onboard buzzer*
J3		

* default

3.8.2 COM2 RS-232/422/485 Select (J4, J6)

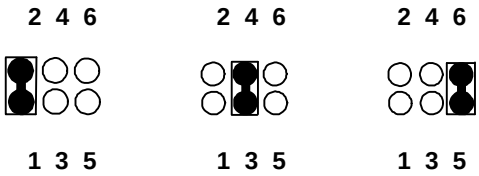
The ECB-875 COM2 serial port can be selected as RS-232, RS-422, or RS-485 by setting J4 & J6.

COM2 RS-232/422/485 Select (J4, J6)			
	RS-232*	RS-422	RS-485
J4			
J6			

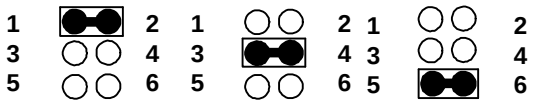
* default

3.8.3 COM1 / 2 Pin 9 Signal Select (J7, J8)

The ECB-875 COM1 / 2 pin 9 signal can be selected as +12V, +5V, or Ring by setting J7 / J8.

COM1 Select (J7)			
	Ring*	+5V	+12V
J7			

* default

COM2 Select (J8)			
	Ring*	+5V	+12V
J8			

* default

3.8.4 Compact Flash Mode Select (J9)

You can use J9 to configure the Compact Flash device to be Master or Slave mode on the secondary IDE channel.

Compact Flash Mode Select (J9)		
	Master*	Slave
J9	1 2	1 2

* default

3.8.5 CPU FSB Frequency Select (J11)

The FSB frequency of CPU can be selected as 100 MHz or auto by J11.

CPU FSB Select (J11)		
	100MHz	Auto*
J11	1 2 3	1 2 3

* default

3.8.6 Clear CMOS (J12)

You can use J12 to clear the CMOS data if necessary. To reset the CMOS data, set J12 to 2-3 closed for just a few seconds, and then remove the jumper back to 1-2 closed.

Clear CMOS (J12)		
	Protect*	Clear CMOS
	1 2 3	1 2 3

* default

3.8.7 M-Systems DiskOnChip Memory Address Select (J13)

The M-systems DiskOnChip memory address can be selected by J13. The choice is D0000~D1FFF, D4000~D5FFF, D8000~D9FFF, or Disabled.

M-systems DiskOnChip Memory Address Select (J13)				
	D0000*	D4000	D8000	Disabled
J13	1 2 3 4	1 2 3 4	1 2 3 4	1 2 3 4

* default

3.9 Connector Definitions

3.9.1 CD-ROM Audio Input Connector (CD_IN1)

Signal	PIN
CD_GND	1
CD_R	2
CD_GND	3
CD_L	4

3.9.2 Signal Description – CD-ROM Audio Input Connector (CD_IN1)

CD L/R	Left and right CD audio input lines.
CD_GND	GND for left and right CD. This GND level is not connected to the board GND.

3.9.3 Pentium IV +12V Connector (CN1)

Signal	PIN			Signal
GND	2		4	+12V
GND	1		3	+12V

3.9.4 External SM Bus Connector (CN2)

Signal	PIN
VCC	4
GND	3
SMBDATA	2
SMBCLK	1

3.9.5 Power Fan Connector (CN3)

SIGNAL	PIN
GND	1
+12V	2
TAC	3

3.9.6 Signal Description – Power Fan Connector (CN3)

TAC	Fan speed monitor

3.9.7 CPU Fan Connector (CN4)

SIGNAL	PIN
GND	1
+12V	2
TAC	3

3.9.8 Signal Description – CPU Fan Connector (CN4)

TAC	Fan speed monitor

3.9.9 Front Panel Connector (CN5)

Signal	PIN		Signal
PW_LED	1	2	GND
VCC	3	4	HD_LED
PWRBTN	5	6	GND
VCC	7	8	BUZZ
RST_SW	9	10	GND
CASEOPEN	11	12	GND

3.9.10 External Standby Power Connector (CN6)

Signal	PIN
POWER_GOOD	1
VCC	2
NC	3
PS_ON	4
GND	5

3.9.11 Primary IDE Connector (CN7)

Signal	PIN		Signal
RESET#	1	2	GND
PDD7	3	4	PDD8
PDD6	5	6	PDD9
PDD5	7	8	PDD10
PDD4	9	10	PDD11
PDD3	11	12	PDD12
PDD2	13	14	PDD13
PDD1	15	16	PDD14
PDD0	17	18	PDD15
GND	19	20	NC
PDDREQ	21	22	GND
PDIOW#	23	24	GND
PDIOR#	25	26	GND
PDIORDY	27	28	IDESEL
PDDACK#	29	30	GND
IRQ14	31	32	NC
PDA1	33	34	CBLID
PDA0	35	36	PDA2
CS0	37	38	CS1
PDDACT#	39	40	GND

3.9.12 Secondary IDE Connector (CN8)

Signal	PIN		Signal
RESET#	1	2	GND
SDD7	3	4	SDD8
SDD6	5	6	SDD9
SDD5	7	8	SDD10
SDD4	9	10	SDD11
SDD3	11	12	SDD12
SDD2	13	14	SDD13
SDD1	15	16	SDD14
SDD0	17	18	SDD15
GND	19	20	NC
SDDREQ	21	22	GND
SDIOW#	23	24	GND
SDIOR#	25	26	GND
SDIORDY	27	28	IDESEL
SDDACK#	29	30	GND
IRQ15	31	32	NC
SDA1	33	34	CBLID
SDA0	35	36	SDA2
CS0	37	38	CS1
SDDACT#	39	40	GND

3.9.13 Signal Description – Primary & Secondary and RAID IDE Connector (CN7, CN8)

PDA [2:0]	**Primary Disk Address [2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector.
SDA [2:0]	**Secondary Disk Address [2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDCS1#	**Primary Disk Chip Select for 1F0H~1F7H Range.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDCS3#	**Primary Disk Chip Select for 3F0H~3F7H Range.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDCS1#	**Secondary Chip Select for 170H~177H Range.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDCS3#	**Secondary Chip Select for 370H~377H Range.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDD [15:0]	**Primary Disk Data [15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDD [15:0]	**Secondary Disk Data [15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

PDIOR#	**Primary Disk IO Read.** In normal IDE this is the command to the IDE device that it may drive data onto the PDD [15:0] lines. Data is latched by PIIX4 on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA [2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDIOR#	**Secondary Disk IO Read.** In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD [15:0] lines. Data is latched by the PIIX4 on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA [2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDIOW#	**Primary Disk IO Write.** In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD [15:0] lines. Data is latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA [2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDIOW#	**Secondary Disk IO Write.** In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD [15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA [2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

PDIORDY	**Primary IO Channel Ready.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. This is a Schmitt triggered input.
SDIORDY	**Secondary IO Channel Ready.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.
PDDREQ	**Primary Disk DMA Request.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDDREQ	**Secondary Disk DMA Request.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDDACK#	**Primary DMA Acknowledge.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.

SDDACK#	**Secondary DMA Acknowledge.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
PDDACT#	**Primary Disk Act.** Signal from Primary IDE device indicating Primary IDE device activity. The signal level depends on the hard disk type, normally active low.
SDDACT#	**Secondary Disk Act.** Signal from Secondary IDE device indicating Secondary IDE device activity. The signal level depends on the hard disk type, normally active low.
RESET#	IDE Reset. This signal resets all the devices that are attached to the IDE interface.
IRQ14/15	Interrupt line from hard disk. Connected directly to PC-AT bus.

3.9.14 Floppy Connector (CN9)

Signal	PIN		Signal
GND	1	2	RWC#
GND	3	4	NC
NC	5	6	DRVDEN1#
GND	7	8	INDEX#
GND	9	10	MOA#
GND	11	12	DSB#
GND	13	14	DSA#
GND	15	16	MOB#
GND	17	18	DIR#
GND	19	20	STEP#
GND	21	22	WD#
GND	23	24	WE#
GND	25	26	TRAK0#
GND	27	28	WPT#
GND	29	30	RDATA#
GND	31	32	SIDE1#
GND	33	34	DSKCHG#

3.9.15 Signal Description – Floppy Connector (CN9)

RDATA#	The read data input signal from the FDD.
WD#	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	Write enable. An open drain output.
MOA#	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
MOB#	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DSA#	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DSB#	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	Direction of the head step motor. An open drain output Logic 1 = outward motion Logic 0 = inward motion
STEP#	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
DRVDEN0#	This output indicates whether a low drive density (250/300kbps at low level) or a high drive density (500/1000kbps at high level) has been selected.
TRAK0#	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
INDEX#	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
WP#	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
DSKCHG#	Diskette change. This signal is active low at power on and whenever the diskette is removed.

3.9.16 Parallel Port Connector (CN10)

Signal	PIN		Signal
STB#	1	2	AFD#
PD0	3	4	ERR#
PD1	5	6	INIT#
PD2	7	8	SLIN#
PD3	9	10	GND
PD4	11	12	GND
PD5	13	14	GND
PD6	15	16	GND
PD7	17	18	GND
ACK#	19	20	GND
BUSY	21	22	GND
PE	23	24	GND
SLCT	25	26	NC

3.9.17 Signal Description – Parallel Port Connector (CN10)

PD [7:0]	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Output line for detection of printer selection. This pin is pulled high internally.
SLCT	An active high input on this pin indicates that the printer is selected. This pin is pulled high internally.
STB#	An active low output is used to latch the parallel data into the printer. This pin is pulled high internally.
BUSY	An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally.
ACK#	An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally.
INIT#	Output line for the printer initialization. This pin is pulled high internally.
AFD#	An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally.
ERR#	An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally.
PE	An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.

3.9.18 Serial Port 2 Connector (CN11)

Signal	PIN		Signal
DCD	1	2	RxD
TxD	3	4	DTR
GND	5	6	DSR
RTS	7	8	CTS
RI	9	10	NC

3.9.19 Serial Port 2 with External DB9 Connector (CN11)

Signal	PIN		Signal
GND	5		
		9	RI
DTR	4		
		8	CTS
TxD	3		
		7	RTS
RxD	2		
		6	DSR
DCD	1		

3.9.20 Signal Description – Serial Port 1 / 2 Connector (CN16, CN11)

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

3.9.21 DVO Port B (CN12)

Signal	PIN		Signal
DVOB_CLK	1	2	DVOB_VSYNC
DVOB_CLK#	3	4	DVOB_HSYNC
GND	5	6	GND
DVOB_D0	7	8	DVOB_D1
DVOB_D2	9	10	DVOB_D3
DVOB_D4	11	12	DVOB_D5
DVOB_D6	13	14	DVOB_D7
DVOB_D8	15	16	DVOB_D9
DVOB_D10	17	18	DVOB_D11
DVOB_BLANK	19	20	DVOB_FLDSTL
GND	21	22	GND
MDVI_DATA	23	24	MI2C_DATA
MDVI_CLK	25	26	MI2C_CLK
MDDC_CLK	27	28	DVOBC_CLKINT#
MDDC_DATA	29	30	DVOBC_INTR#
ADD_DETECT	31	32	RESET#
+12V	33	34	+12V
VCC3	35	36	VCC3
VCC	37	38	VCC
GND	39	40	GND

3.9.22 DVO Port C (CN13)

Signal	PIN		Signal
DVOC_CLK	1	2	DVOC_VSYNC
DVOC_CLK#	3	4	DVOC_HSYNC
GND	5	6	GND
DVOC_D0	7	8	DVOC_D1
DVOC_D2	9	10	DVOC_D3
DVOC_D4	11	12	DVOC_D5
DVOC_D6	13	14	DVOC_D7
DVOC_D8	15	16	DVOC_D9
DVOC_D10	17	18	DVOC_D11
DVOC_BLANK	19	20	DVOC_FLDSTL
GND	21	22	GND
MDVI_DATA	23	24	MI2C_DATA
MDVI_CLK	25	26	MI2C_CLK
MDDC_CLK	27	28	DVOBC_CLKINT#
MDDC_DATA	29	30	DVOBC_INTR#
ADD_DETECT	31	32	RESET#
+12V	33	34	+12V
VCC3	35	36	VCC3
VCC	37	38	VCC
GND	39	40	GND

Note:

Optional daughter board is available.

3.9.23 Signal Description – DVO port B & DVO port C (CN12, CN13)

DVOB_CLK; DVOB_CLK#	O AGP	**DVOB Clock Output**: These signals provide a differential pair reference clock that can run up to 165 MHz. Formerly known by: DVOB_CLKOUT0=DVOB_CLK and DVOB_CLKOUT1=DVOB_CLK#. Care should be taken to be sure that DVOB_CLK is connected to the primary clock receiver of the Intel ® DVO device.
DVOB_D[11:0]	O AGP	**DVOB Data**: This data bus is used to drive 12-bit pixel data on each edge of DVOB_CLK (#). This provides 24 bit of data per clock.
DVOB_HSYNC	O AGP	**Horizontal Sync:** This is the HYNC signal for the DVOB interface. The active polarity of the signal is programmable.
DVOB_VSYNC	O AGP	**Vertical Sync:** This is the VSYNC signal for the DVOB interface. The active polarity of the signal is programmable.
DVOB_BLANK#	O AGP	**Flicker Blank or Border Period Indication:** DVOB_BLANK# is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels.
DVOBC_CLKINT#	I AGP	**DVOBC Pixel Clock Input/Interrupt:** This signal may be selected as the reference input to the dot clock PLL (DPLL) for the multiplexed DVO devices. This pin may also be programmed to be an interrupt input for either of the multiplexed DVO devices.
DVOB_FLDSTL#	I AGP	**TV Field and Flat Panel Stall Signal:** This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. When used as a Field input, it synchronizes the overlay field with the TV encoder field when overlay is displaying an interleaved source. When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The polarity is programmable for both modes and the input may be disabled completely.
DVOC_CLK; DVOC_CLK#	O AGP	**DVOC Clock Output**: These signals provide a differential pair reference clock that can run up to 165 MHz. Formerly known by: DVOC_CLKOUT0=DVOC_CLK and DVOC_CLKOUT1=DVOC_CLK#. Care should be taken to be sure that DVOC_CLK is connected to the primary clock receiver of the Intel ® DVO device.
DVOC_D[11:0]	O AGP	**DVOC Data**: This data bus is used to drive 12-bit pixel data on each edge of DVOC_CLK (#). This provides 24 bit of data per clock.
DVOC_HSYNC	O AGP	**Horizontal Sync:** This is the HYNC signal for the DVOC interface. The active polarity of the signal is programmable.

DVOC_VSYNC	O AGP	**Vertical Sync:** This is the VSYNC signal for the DVOC interface. The active polarity of the signal is programmable.
DVOC_BLANK#	O AGP	**Flicker Blank or Border Period Indication:** DVOC_BLANK# is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels.
DVOBC_INTR#	I AGP	**DVOBC Interrupt:** This signal may be used as an interrupt input for either of the multiplexed DVO devices.
DVOC_FLDSTL#	I AGP	**TV Field and Flat Panel Stall Signal:** This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. When used as a Field input, it synchronizes the overlay field with the TV encoder field when overlay is displaying an interleaved source. When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The polarity is programmable for both modes and the input may be disabled completely.
MI2C_CLK	I/O AGP	**MI2C_CLK**: The specific function of the signal is I2C_CLK for a multiplexed digital display. This signal is tri-stated during a hard reset.
MI2C_DATA	I/O AGP	**MI2C_DATA**: The specific function of the signal is I2C_DATA for a multiplexed digital display. This signal is tri-stated during a hard reset.
MDVI_CLK	I/O AGP	**MDVI_CLK**: The specific function is DVI_CLK (DDC) for a multiplexed digital display connector. The signal is tri-stated during a hard reset.
MDVI_DATA	I/O AGP	**MDVI_DATA**: The specific function is DVI_DATA (DDC) for a multiplexed digital display connector. The signal is tri-stated during a hard reset.
MDDC_CLK	I/O AGP	**MDDC_CLK**: This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector. This signal is tri-stated during a hard reset.
MDDC_DATA	I/O AGP	**MDDC_DATA**: This signal may be used as the DDC_Data for a secondary multiplexed digital display connector. This signal is tri-stated during a hard reset.
ADDID[7:0]	I/O AGP	**ADD Card ID**: These signals will be strapped on the ADD card for software identification purposes. These signals may need pull-up or pull-down resistors in a DVO device down scenario.
RESET	Pin 32	**Reset:** Active low reset signal during power-up or from the control register.

3.9.24 Audio Output Connector (CN14)

Signal	PIN		Signal
Line-Out R	1	2	Line-Out L
AGND	3	4	AGND
Line-In R	5	6	Line-In L
Mic	7	8	AREF
SPK R	9	10	SPK L

3.9.25 Daughter Board Connector A (CN15)

Signal	PIN		Signal
USBP3P B	1	2	USBP2P B
USBP3N B	3	4	USBP2N B
USBV4	5	6	USBV3
USBG1	7	8	USBG0
USBP1P B	9	10	USBP0P B
USBP1N B	11	12	USBP0N B
USBV2	13	14	USBV1
USBG1	15	16	USBG0
VCCSB	17	18	SLED2
LLED2	19	20	ALED2

3.9.26 Daughter Board Connector B (CN21)

Signal	PIN		Signal
LAN_CLK	1	2	LAN_RXD0
LAN_RSTSYNC	3	4	LAN_RXD1
VCC	5	6	LAN_RXD2
NC	7	8	LAN_TXD0
NC	9	10	LAN_TXD1
NC	11	12	LAN_TXD2
TDPB	13	14	GND
RDPB	15	16	TDNB
MDAT	17	18	RDNB
MCLK	19	20	VCC

Note:

Optional daughter board is available.

3.9.27 IrDA Connector (CN17)

Signal	PIN
VCC	1
NC	2
IRRX	3
GND	4
IRTX	5

3.9.28 Signal Configuration –IrDA Connector (CN17)

IRRX	Infrared Receiver input
IRTX	Infrared Transmitter output

3.9.29 10/100 BASE-Tx Ethernet Connector (CN19)

Signal	PIN
TxD+	1
TxD-	2
RxD+	3
NC	4
NC	5
RxD-	6
NC	7
NC	8

3.9.30 Signal Description – 10/100Base-Tx Ethernet Connector (CN19)

TXD+ / TXD-	Ethernet 10/100Base-Tx differential transmitter outputs.
RXD+ / RXD-	Ethernet 10/100Base-Tx differential receiver inputs.

3.9.31 USB Connector (CN20)

Signal	PIN		Signal
	CH1	CH2	
VCC	1	2	VCC
D0-	3	4	D1-
D0+	5	6	D1+
GND	7	8	GND
NC	9	10	NC

3.9.32 Signal Description – USB Connector (CN20)

D0+ / D0-	Differential bi-directional data signal for USB channel 0. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
D1+ / D1-	Differential bi-directional data signal for USB channel 1. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
VCC	5 V DC supply for external devices. Maximum load according to USB standard.

3.9.33 VGA Connector (CN22)

Signal	PIN			Signal
		6		ANA-GND
RED	1		11	NC
		7		ANA-GND
GREEN	2		12	DDCDAT
		8		ANA-GND
BLUE	3		13	HSYNC
		9		VCC
NC	4		14	VSYNC
		10		DIG-GND
DIG-GND	5		15	DDCCLK

3.9.34 Signal Description – VGA Connector (CN22)

HSYNC	CRT horizontal synchronisation output.
VSYNC	CRT vertical synchronisation output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 0 cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 0 cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 0 cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

3.9.35 Power Connector (CN23)

SIGNAL	PIN
+12V	1
GND	2
GND	3
+5V	4

3.9.36 Chassis Fan Connector (CN24)

SIGNAL	PIN
TAC	3
+12V	2
GND	1

3.9.37 Signal Description – Chassis Fan Connector

TAC	Fan speed monitor

3.9.38 North Bridge Fan Connector (CN25)

SIGNAL	PIN
GND	1
VCC	2

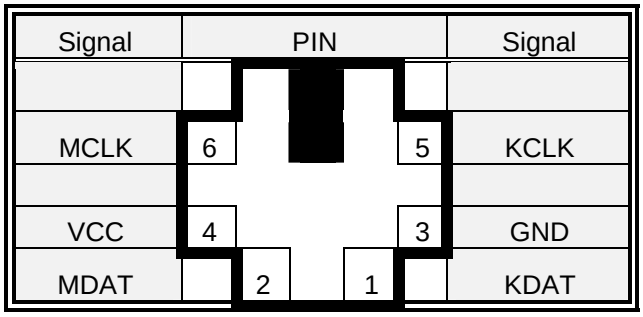
3.9.39 Internal Keyboard Connector (CN26)

Signal	PIN
KCLK	1
KDAT	2
NC	3
GND	4
VCC	5

3.9.40 Signal Description – Internal Keyboard Connector (CN26)

KCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

3.9.41 PS/2 Keyboard & Mouse Connector (CN27)



3.9.42 Signal Description – PS/2 Keyboard & Mouse Connector (CN27)

MCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.

3.9.43 Auxiliary Power Connector (J2)

Signal	PIN
PSON#	1
VCC	2
VCCSB	3

Note:

Set J2 to 2-3 closed. If AT power supply is to be used.

4. Award BIOS Setup

4.1 Starting Setup

The AwardBIOS™ is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing <Del> immediately after switching the system on, or

By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

```
Press DEL to enter SETUP
```

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

```
Press F1 To Continue, DEL to enter SETUP
```

4.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item in the left hand
Right arrow	Move to the item in the right hand
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

Table 1 Legend Keys

4.2.1 Navigating through the menu bar

Use the left and right arrow keys to choose the menu you want to be in.

4.2.2 To display a sub menu

Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A "➢" pointer marks all sub menus.

4.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

4.4 In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

4.5 Main Menu

Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

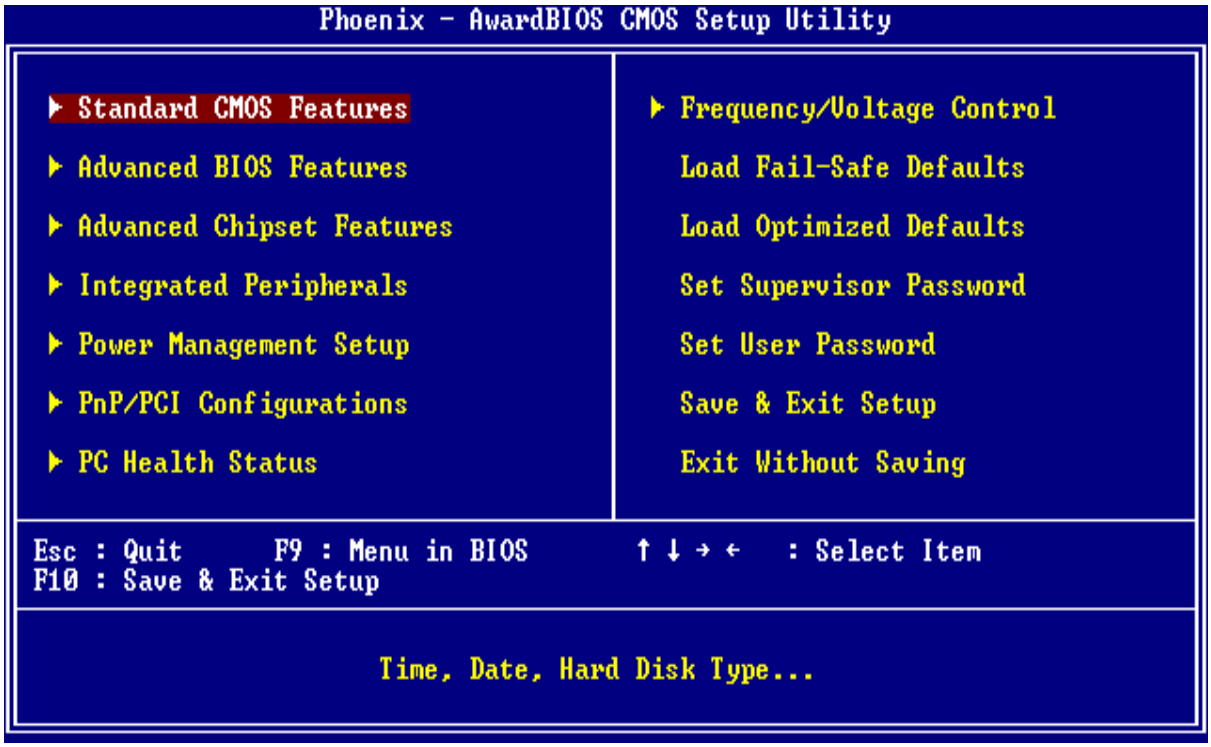


Figure 1: The Main Menu

Note:

It is strongly recommended to reload Optimized setting if CMOS is lost or BIOS is updated.

4.5.1 Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

4.5.1.1 Standard CMOS Features

Use this menu for basic system configuration.

4.5.1.2 Advanced BIOS Features

Use this menu to set the Advanced Features available on your system.

4.5.1.3 Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system's performance.

4.5.1.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

4.5.1.5 Power Management Setup

Use this menu to specify your settings for power management.

4.5.1.6 PNP / PCI Configuration

This entry appears if your system supports PnP / PCI.

4.5.1.7 Frequency / Voltage Control

Use this menu to specify your settings for frequency/voltage control.

4.5.1.8 Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

4.5.1.9 Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

4.5.1.10 Supervisor / User Password

Use this menu to set User and Supervisor Passwords.

4.5.1.11 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

4.5.1.12 Exit Without Save

Abandon all CMOS value changes and exit setup.

4.5.2 Standard CMOS Setup

The items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.

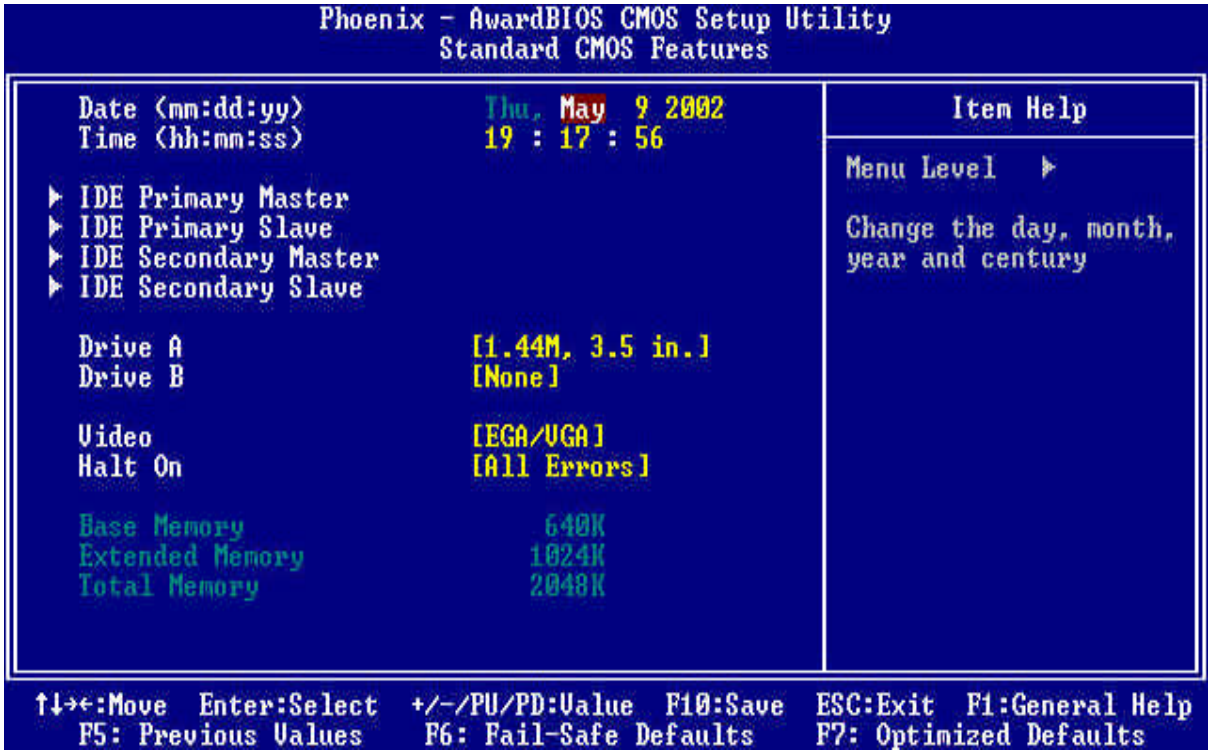


Figure 2: The Standard CMOS Features

4.5.2.1 Standard CMOS Selection

This table shows the selections that you can make on the Standard CMOS Selection.

Item	Options	Description
Date	Month DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
IDE Primary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Primary Slave	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
Drive A Drive B	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you
Base Memory	N/A	Displays the amount of conventional memory detected during boot up
Extended Memory	N/A	Displays the amount of extended memory detected during boot up
Total Memory	N/A	Displays the total memory available in the system

Table 2 The Standard CMOS Features Selections

4.5.2.2 IDE Adapters

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive.

Figure 2 shows the IDE primary master sub menu.

Use the legend keys to navigate through this menu and exit to the main menu. Use Table 3 to configure the hard disk.

Item	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Capacity	Auto Display your disk drive size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
Access Mode	Normal LBA Large Auto	Choose the access mode for this hard disk
The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'		
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** **Warning**: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

Table3 Hard disk selections

4.5.3 Advanced CMOS Setup Defaults

This Setup includes all of the advanced features in the system. The detail descriptions are specified as below.

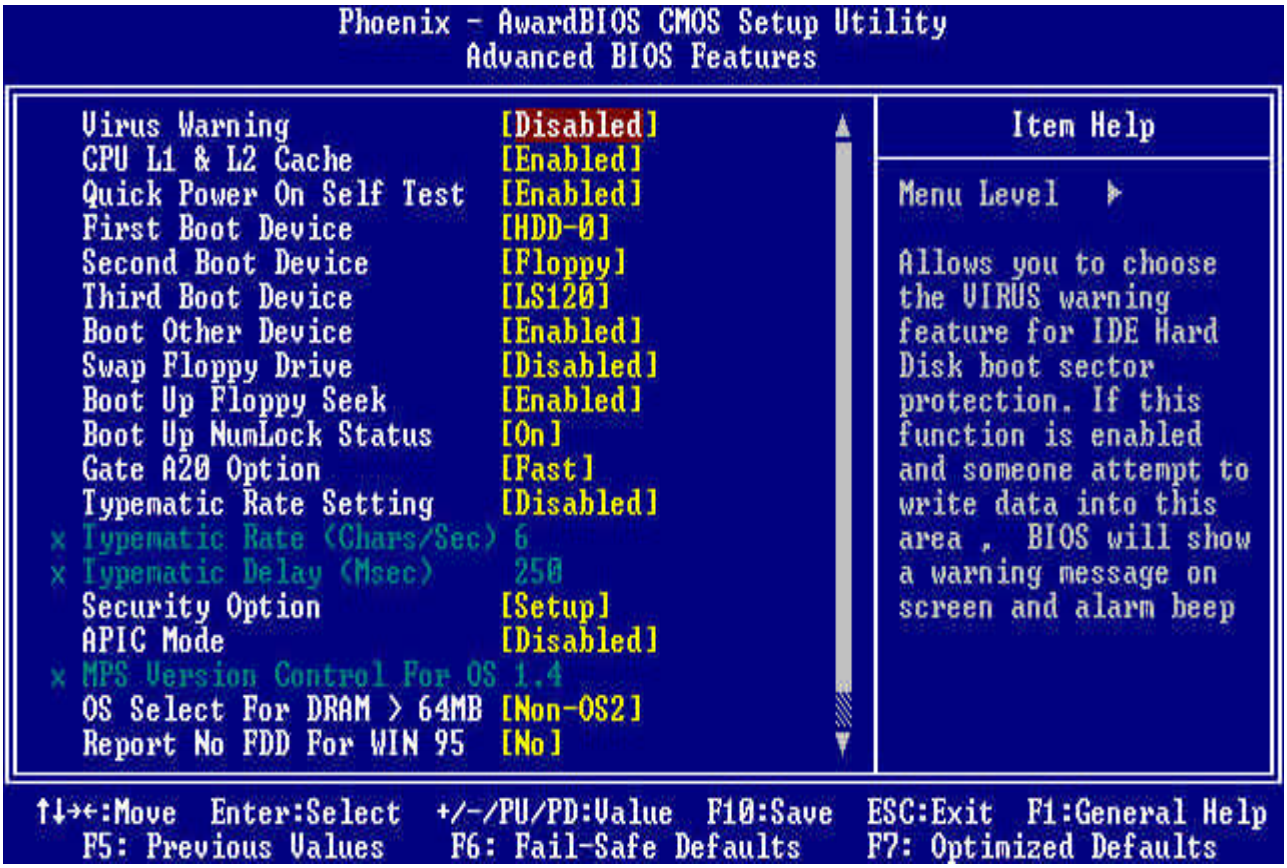


Figure 3: The Advanced CMOS Features

4.5.3.1 Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

4.5.3.2 CPU Internal Cache/External Cache

These two categories speed up memory access. However, it depends on CPU/chipset design.

Enabled	Enable cache
Disabled	Disable cache

4.5.3.3 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enable quick POST
Disabled	Normal POST

4.5.3.4 First/Second/Third/Other Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

The Choice: Floppy, LS/ZIP, HDD, SCSI, CDROM, and Disabled.

4.5.3.5 Swap Floppy Drive

If the system has two floppy drives, you can swap the logical drive name assignments.

The choice: Enabled/Disabled.

4.5.3.6 Boot Up Floppy Seek

Seeks disk drives during boot up. Disabling speeds boot up.

The choice: Enabled/Disabled.

4.5.3.7 Boot Up NumLock Status

Select power on state for NumLock.

The choice: Enabled/Disabled.

4.5.3.8 Gate A20 Option

Select if chipset or keyboard controller should control GateA20.

Normal	A pin in the keyboard controller controls GateA20
Fast	Lets chipset control GateA20

4.5.3.9 Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

The choice: Enabled/Disabled.

4.5.3.10 Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a key stroke when you hold the key down.

The choice: 6, 8, 10, 12, 15, 20, 24, 30.

4.5.3.11 Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke.

The choice: 250, 500, 750, and 1000.

4.5.3.12 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

4.5.3.13 APIC Mode

The BIOS supports versions 1.4 of the Intel multiprocessor specification. When enabled, The MPS Version 1.4 Control for OS can be activated.

The choice: Enabled/Disabled.

4.5.3.14 OS Select for DRAM > 64

Select the operating system that is running with greater than 64MB of RAM on the system.

The choice: Non-OS2, OS2.

4.5.3.15 Report No FDD for Win 95

While the FDD in " STANDARD CMOS SETUP " is set to NONE, set this option to No to release IRQ6 for passing Win95 logo. This option is irrelevant under normal operation.

The choice: Yes, No.

4.5.3.16 Small Logo (EPA) Show

When you select " Enabled" the screen shows as "Energy Star" picture at the front side up right. "Disabled" is close this picture.

The choice: Enable, Disable.

4.5.4 Advanced Chipset Setup Defaults

This Setup is very important to keep system's stability. If you are not technical person, do not attempt to change any parameters. The best way is to choose optimal default setting.

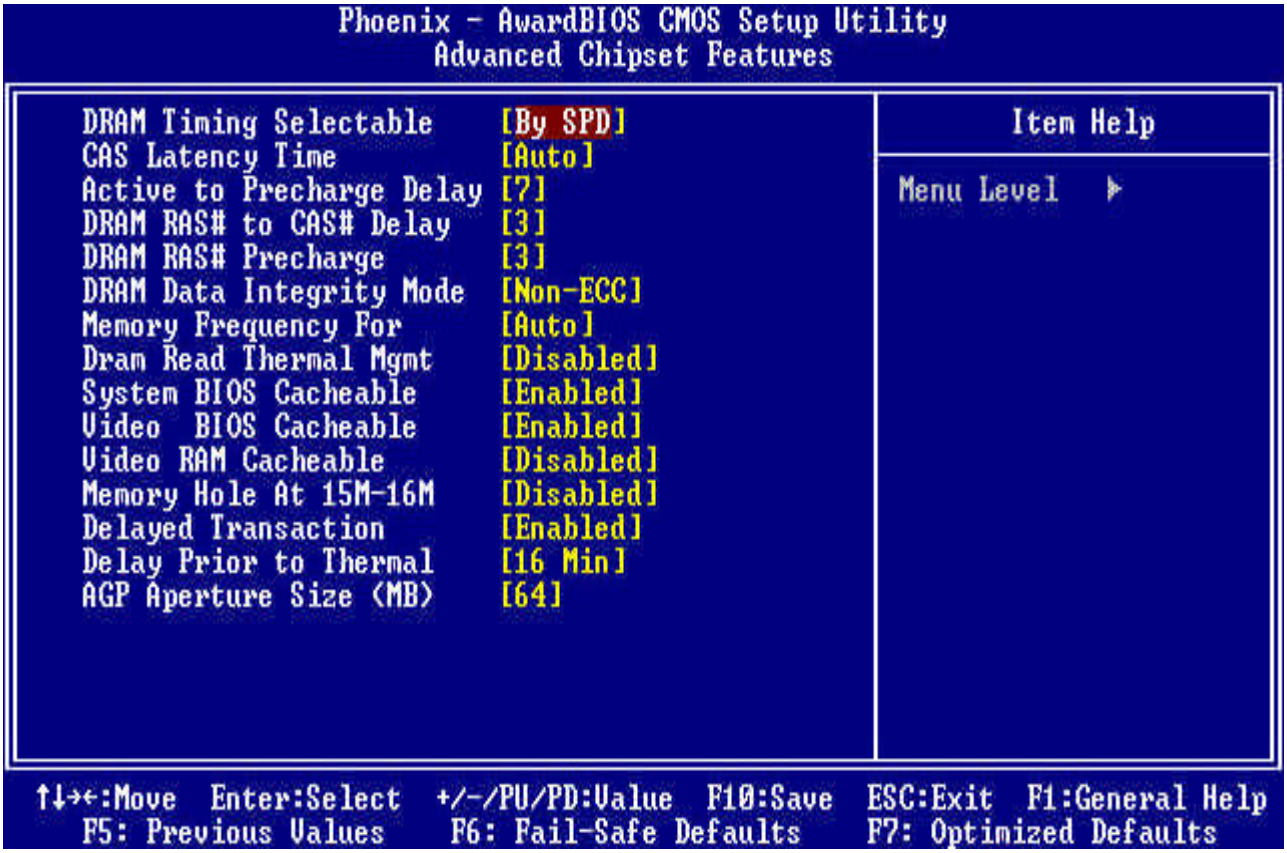


Figure 4: The Advanced Chipset Features

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.

4.5.4.1 DRAM Timing Selectable

If your DIMM memory has SPD (Serial Presence Detect) 8-pin IC on module, you can set this option to "By SPD". System will set your SDRAM clock and timing from the SPD IC. If the option set as "Manual", DRAM clock and timing must be set from items below:

The choice: SPD, Manual.

4.5.4.2 SDRAM CAS Latency Time

When synchronous DRAM is installed, the number of clock cycles of CAS latency depends on the DRAM timing. Do not reset this field from the default value specified by the system designer. This controls the latency between the SDRAM read command and the time that the data actually becomes available.

The choice: 1.5, 2, 2.5, 3, and Auto.

4.5.4.3 Active to Precharge delay

When you select "Manual" mode, you can set active to Precharge SDRAM timing delay.

The choice: 7, 6, 5, and Auto.

4.5.4.4 SDRAM RAS-to-CAS Delay

These are timing of SDRAM CAS Latency and RAS to CAS Delay, calculated by clocks. They are important parameters affects SDRAM performance.

The choice: 3, 2.

4.5.4.5 SDRAM RAS Precharge Time

The RAS Recharge means the timing to inactive RAS and the timing for DRAM to do recharge before next RAS can be issued.

The choice: 3, 2.

4.5.4.6 Memory Frequency For

When you select "Auto" mode, Allows DRAM PC 100 or PC 133 Data Integrity mode.

The choice: PC100, PC133, Auto.

4.5.4.7 DRAM Read Thermal Mgmt.

When you select "Manual" mode, you can set DRAM Read Thermal Mgmt.

The choice: Enable, Disable.

4.5.4.8 System BIOS Cacheable

Allows the system BIOS to be cached for faster system performance.

The choice: Enable, Disable.

4.5.4.9 Video BIOS Cacheable

Allows the video BIOS to be cached for faster video performance.

The choice: Enable, Disable.

4.5.4.10 Video RAM Cacheable

Allows the video RAM to be cached for faster video performance.

The choice: Enable, Disable.

4.5.4.11 Memory Hole At 15M-16M

Enabling this feature reserves 15MB to 16MB memory address space to ISA expansion cards that specifically require this setting. This makes the memory from 15MB and up unavailable to the system. Expansion cards can only access memory up to 16MB.

The choice: Enable, Disable.

4.5.4.12 Delayed Transaction

This function is used to meet the latency of PCI cycles to from ISA bus. Try to enable or disable it, if you have ISA card compatibility problem.

The choice: Enable, Disable.

4.5.4.13 Delay Prior to Thermal

When you system temperature higher, you can set the DRAM access time slowdown between on 4 min – 32 min delay.

The choice: 4 Min, 8 Min, 16 Min, and 32 Min.

4.5.4.14 AGP Aperture Size (MB)

Choose 32, 64MB. Memory-mapped, graphics data structures can reside in the Graphics Aperture.

The choice: 4 , 8, 16, 32, 64, 128 and 256.

4.5.5 Integrated Peripherals Setup Defaults

This section describes I/O resources assignment for all of on-board peripheral devices.

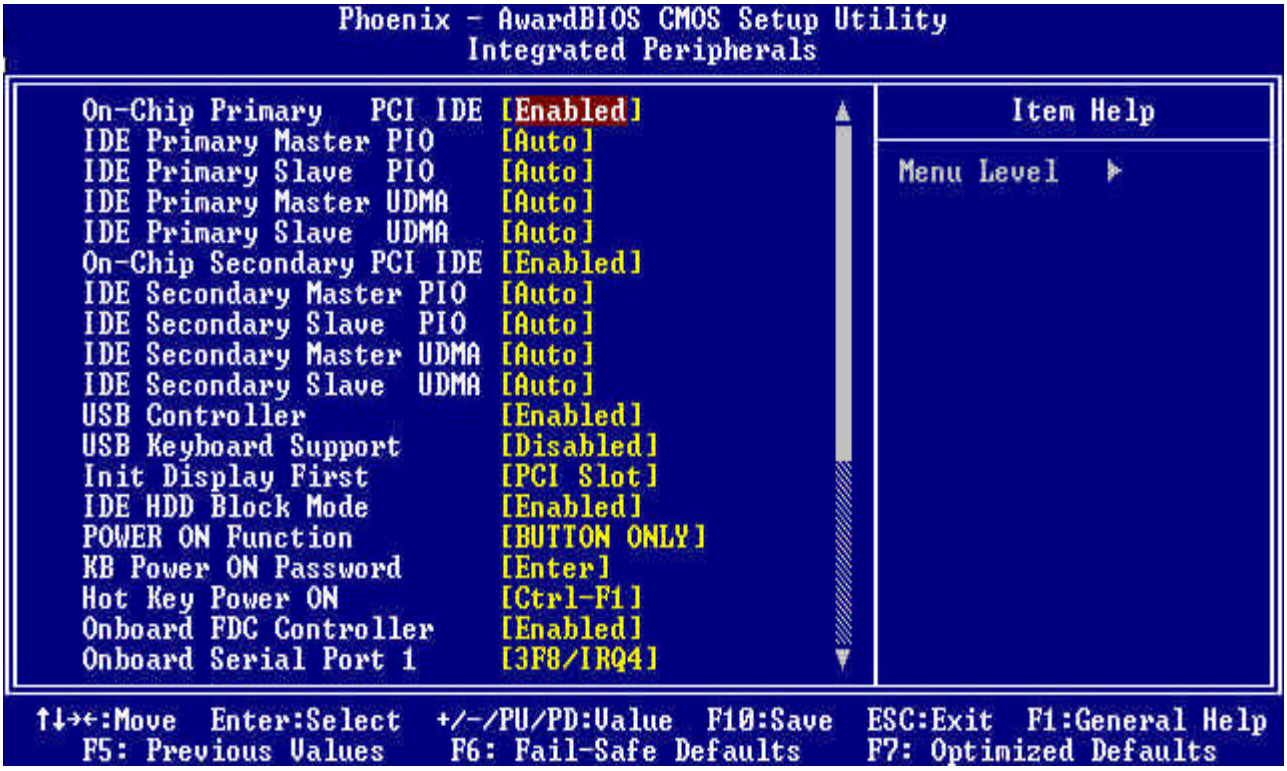


Figure 5: The Integrated Peripherals Features

4.5.5.1 On-Chip Primary/Secondary PCI IDE

Select "Enabled" to activate each on-board IDE channel separately, Select "Disabled", if you install an add-on IDE Control card.

The choice: Enable, Disable.

4.5.5.2 IDE Primary & Secondary Master/Slave PIO

These four PIO fields let you set a PIO mode (0-4) for each of four IDE devices. When under "Auto" mode, the system automatically set the best mode for each device.

The choice: Auto, Mode 0, Mode 1, Mode 2, Mode 3, and Mode 4.

4.5.5.3 IDE Primary & Secondary Master/Slave UDMA

When set to "Auto" mode, the system will detect if the hard drive supports Ultra DMA mode.

The choice: Auto, Mode 0, Mode 1, Mode 2, Mode 3, and Mode 4.

4.5.5.4 USB Controller

Select Enabled if your system contains a Universal Serial Bus (USB) controller.

The choice: Enable, Disable.

4.5.5.5 USB Keyboard Support

This item lets you enable or disable the USB keyboard driver within the onboard BIOS.

The choice: Enable, Disable.

4.5.5.6 Init Display First

Select “AGP” or “PCI Slot” for system to detect first when boot-up.

The choice: PCI Slot, AGP.

4.5.5.7 IDE HDD Block Mode

This feature enhances disk performance by allowing multi-sector data transfers and eliminates the interrupt handling time for each sector.

The choice: Enable, Disable.

4.5.5.8 POWER ON Function

This field allows you to use the keyboard to power-on the system. Use Table 3 to configure this function.

Item	Options	Description
Password	Press Enter	When this option is selected, move the cursor to the "KB Power On Password" field and press <Enter>. Enter your password. You can enter up to 5 characters. Type in exactly the same password to confirm, then press <Enter>.
Hot Key	Ctrl-F1 to Ctrl-F12	When this option is selected, move the cursor to the " Hot Key Power On " field to select a function key you would like to use to power-on the system. The options are from Ctrl-F1 to Ctrl-F12.
Any Key	Press Enter	Press any key to power-on the system,
Mouse Left	Press Enter	When this option is selected, double-click the left button of the mouse to power-on the system.
Mouse Right	Press Enter	When this option is selected, double-click the right button of the mouse to power-on the system.
Button Only	Press Enter	System can be power on with Power Button.
Keyboard 98	Press Enter	When this option is selected, press the "wake up" key of the Windows 98 compatible keyboard to power-on the system.

Table4 Power On function selections

4.5.5.9 Onboard FDC Controller

Select “Enabled” to activate the on-board FDC and “Disabled” to activate an add-on FDC.

The choice: Disable, Enable.

4.5.5.10 Onboard Serial Port 1 & 2

Select an address and corresponding interrupt for the first/second serial port. The default value for the first serial port is “3F8/IRQ4” and the second serial port is “2F8/IRQ3”.

The choice: Disable, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 3F8/IRQ3, and Auto.

4.5.5.11 UART Mode Select

Select to activate the Infrared transfer function.

The choice: IrDA, ASKIR, Normal.

4.5.5.12 RxD , TxD Active

This choice: Hi, Lo; Lo, Hi; Lo, Lo; Hi, Hi.

4.5.5.13 IR Transmission Delay

If this option is enabled, transmission of data will be slower. This is recommended when you encounter transmission problem with your device.

The choice: Disable, Enable.

4.5.5.14 UR2 Duplex Mode

Select to activate the Infrared transfer function. This default setting is “Half“.

The choice: Full, Half.

4.5.5.15 Use IR Pin

When you select to IrDA or ASKIR mode, you can define use (TX,RX) pin.

The choice: RxD2, TxD2; IR-Rx2Tx2.

4.5.5.16 Onboard Parallel Port

Select address and interrupt for the Parallel port.

The choice: Disable, 378/IRQ7, 278/IRQ5, and 3CB/IRQ7.

4.5.5.17 Parallel Port Mode

Select an operating mode for the parallel port.

The choice: SPP, EPP, ECP, ECP+EPP, and Normal.

4.5.5.18 EPP Mode Select

Set parallel port as EPP1.7 or EPP1.9.

The choice: EPP1.7, EPP1.9.

4.5.5.19 ECP Mode Use DMA

Select a DMA channel if parallel port is set as ECP or ECP+EPP.

The choice: 1, 3.

4.5.5.20 PWRON After PWR-Fail

Select the option for the system action after an AC power failure.

Off	When power returns after an AC power failure, the system's power is off. You must press the Power button to power-on the system.
On	When power returns after an AC power failure, the system will automatically power-on.
Former-Sts	When power returns after an AC power failure, the system will return to the state where you left off before power failure occurs. If the system's power is off when AC power failure occurs, it will remain off when power returns. If the system's power is on when AC power failure occurs, the system will power-on when power returns.

4.5.6 Power Management Setup Defaults

This APM (Advanced Power Management) determines how much power energy setting below items to handle system power resource can save. The following descriptions will specify the definition of each item in details.

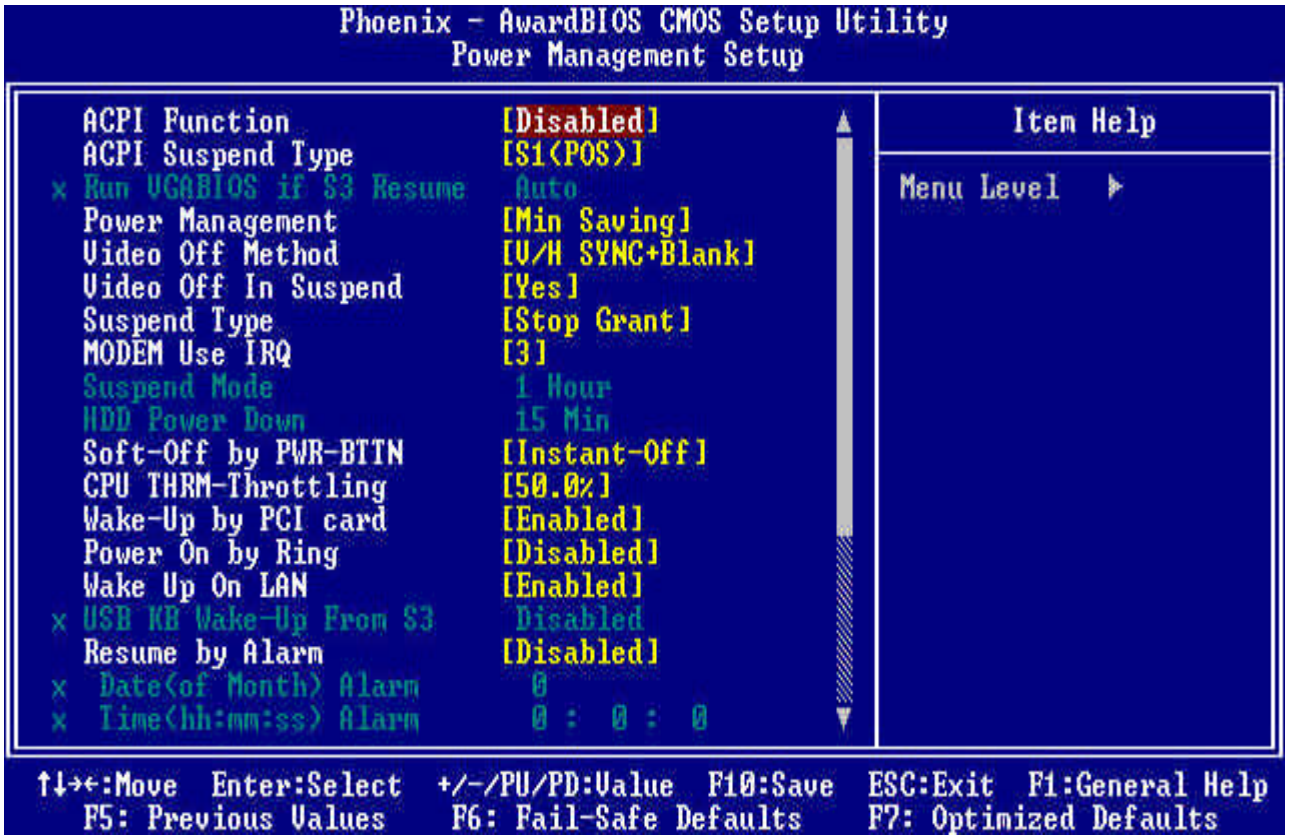


Figure 6: The Power Management Setup

4.5.6.1 ACPI Function

This item allows you to enable or disable the function of Advanced Configuration and Power Interface (ACPI) that offers improved power management.

The choice: Disable, Enable.

4.5.6.2 ACPI Suspend Type

This field is used to select the type of Suspend function.

S1 (POS)	Enables the Power On Suspend function.
S3 (STR)	Enables the Suspend to RAM function. Refer to Appendix A.
S1&S3	Enables the Power On Suspend function and Enables the Suspend to RAM function. Refer to Appendix A.

4.5.6.3 VGABIOS if S3 Resume

When select S3 or S1&S3 can conveniently Enables VGA BIOS, Suspend to RAM function and Power On Suspend function.

The choice: Auto, Yes, No.

4.5.6.4 Power Management

Mini Saving	System starts power saving function when the inactivity period exceeds 1 hour.
Max Saving	System starts power saving function when the inactivity period exceeds 1 min.
User Defined	Allows user to define the inactivity period before power saving function activates,

4.5.6.5 Video Off Method

This field defines the video off features. The following options are available: DPMS OFF, DPMS Reduce ON, Blank Screen, V/H SYNC+Blank, DPMS Standby, and DPMS Suspend. The DPMS (Display Power Management System) features allow the BIOS to control the video display card if it supports the DPMS feature.

The choice: Blank Screen, V/H SYNC+Blank, DPMS.

4.5.6.6 Video Off In Suspend

This option is used to activate the video off feature when the system enter the suspend mode.

The choice: Yes, No.

4.5.6.7 Suspend Type

System further shuts down all devices and all right select stop Grant or Power on suspend function.

The choice: stop Grant , PowOn Suspend.

4.5.6.8 MODEM Use IRQ

This item tells the Power Management BIOS which IRQ is assigned to the installed MODEM.

The choice: NA, 3, 4, 5, 7, 9, 10 and 11.

4.5.6.9 Suspend Mode

System further shuts down all devices except for CPU itself. This is the third level of Power Management.

4.5.6.10 HDD Power Down

This instructs hard drives to shut off while in the Power Management modes.

4.5.6.11 Soft-Off by PWR-BTTN

When set to "Delay 4 Sec.", the power button has a dual function where pressing less than 4 seconds will place the system in sleep mode and shut down the system when the button is held more than 4 seconds. "Instant-Off", the system will be shut down right away when the power button is pressed.

The choice: Instant-Off, Delay 4 Sec.

4.5.6.12 CPU Thermal-Throttling

Set the percent of power consumption when CPU over heat.

The choice: 87.5%, 75.0%, 62.5%, 50.0%, 37.5%, 25.0%, 12.5%.

4.5.6.13 Wake-Up by PCI card

If your PCI card supports PME (Power Management Event) signal and this item is set as Enabled, PCI peripherals drive PME signal to wake the system from low-power states S1-S5.

The choice: Disable, Enable.

4.5.6.14 Power On by Ring

The option lets you specify enable or disable external Modem Wake Up function. It powers up the computer when the modem receives a call while the computer is in Soft-off mode.

The choice: Disable, Enable.

> **Note:**
>
> The computer cannot receive or transmit data until the computer and application are fully running. After the item is set as enabled, the system must enter to OS once before system is turned off.

4.5.6.15 Wake up on LAN

This allows you to remotely power up your systems through your network by sending a wake-up frame or signal. With this feature, you can remotely upload/download data to/from systems during off-peak hours. Set to Enabled to set this feature. Please refer to session 2.4.6 for more information.

The choice: Disable, Enable.

4.5.6.16 USB KB Wake-up From S3

If your USB KB supports PME (Power Management Event) signal and this item is set as Enabled, USB KB peripherals drive PME signal to wake the system from low-power states S3.

The choice: Disable, Enable.

4.5.6.17 Resume by Alarm

Set this option to enable or disable the RTC Alarm to Wake Up the system, which is set at soft off.

The choice: Disable, Enable.

4.5.6.18 Date (of Month) Alarm, Time (hh:mm:ss) Alarm

Alarm time on Date / Hour / Minute / Second.Set these options to specify the RTC

4.5.6.19 Primary/Secondary IDE 0/1, FDD, COM, LPT Port & PCI PIRQ [A-D]

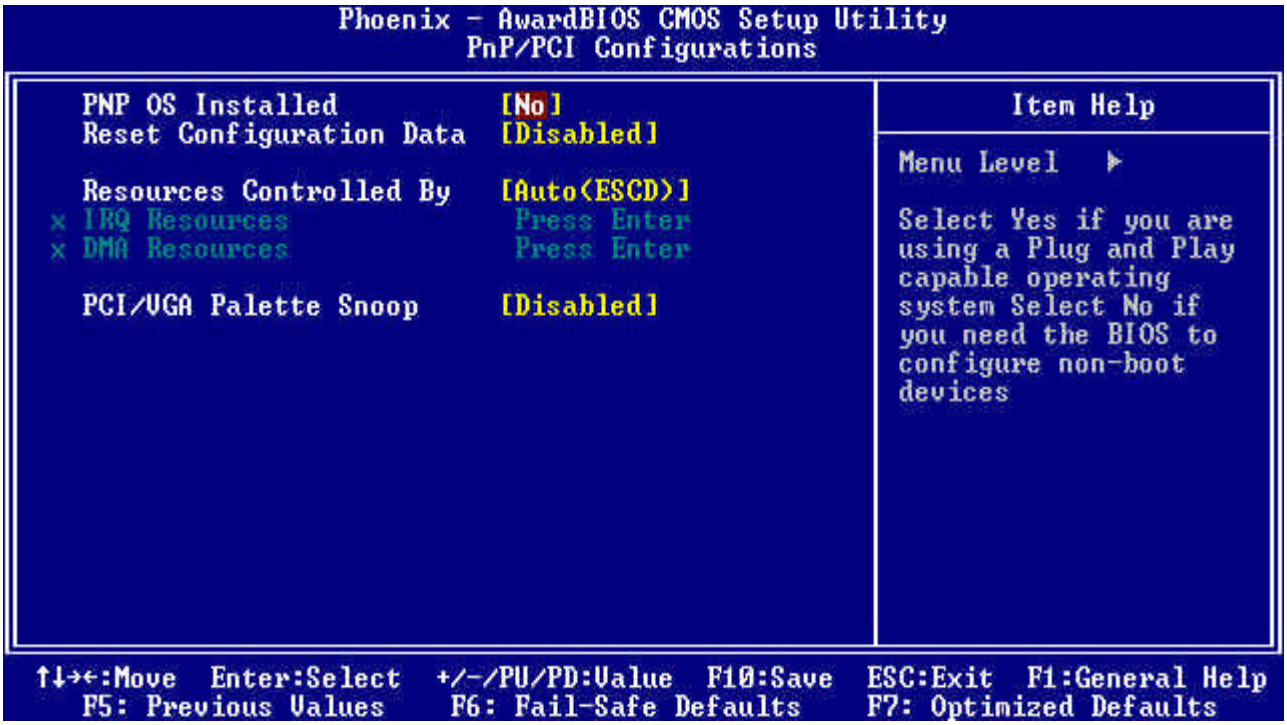
These items enable or disable the detection of IDE, floppy, serial, parallel port and PCI PIRQ [A-D] activities for power down state transition. Actually it detects the read/write to/from I/O port.

The choice: Disable, Enable.

4.5.7 PnP/ PCI Setup Defaults

This section describes configuring the PCI bus system. PCI (Peripheral Component Interconnect) is a system that allows I/O devices to operate at speeds nearing CPU's when they communicate with own special components.

All of options described in this section are important and technical and it is strongly recommended that only experienced users could make any changes to the default settings.



4.5.7.1 PNP OS installed

This field allows you to use a Plug-and-Play (PnP) operating system.

Please set it as "No " if the operating system has no PnP function or to avoid reassigning the IRQs by the operating system.

The choice: Yes, No.

4.5.7.2 Reset Configuration Data

In case a conflict occurs after you assign the IRQs or after you configure your system, you can enable this function to allow your system to automatically reset your configuration and reassign the IRQs, DMAs, and I/O address.

The choice: Disable, Enable.

4.5.7.3 Resources Controlled By

Default setting is “Auto (ESCD)”. This setting allows the BIOS to self detect setting and Plug-and-Play devices during start up. The user can select and configure IRQs under "Manual" mode.

The choice: Auto (ESCD), Manual.

4.5.7.4 IRQ Resources

These options specify the bus that the named interrupt request lines (IRQs) are used on. These options allow you to specify IRQs for use by legacy ISA adapter cards. These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the IRQ by assigning the option to the *ISA/EISA* setting. Onboard I/O is configurable by AMIBIOS. The IRQs used by onboard I/O are configured as *PCI/PnP.* The settings are *PCI/PnP* or *ISA/EIS*A. The default settings are *PCI/Pn*P.

4.5.7.5 DMA Resources

Select the devices according to your DMA requirements

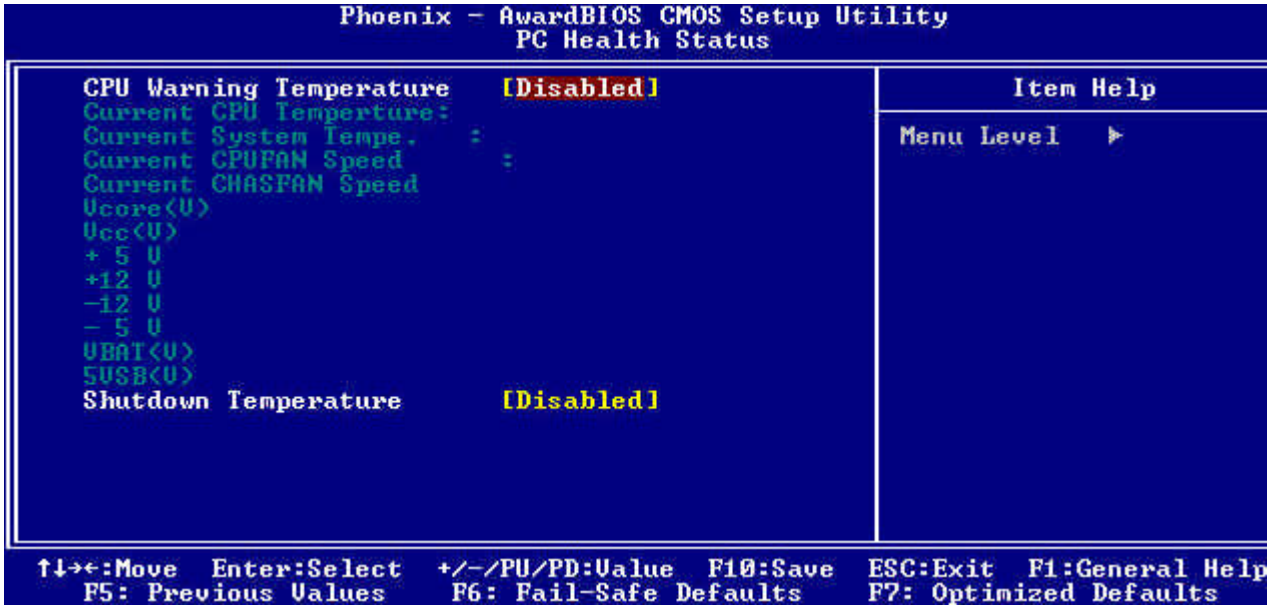
4.5.7.6 PCI/VGA Palette Snoop

Enable this option to correct screen color shifts, when there is a combination of VGA cards, accelerator cards, or MPEG cards present.

The choice: Disable, Enable.

4.5.8 PC Health Status Setup Defaults

This setup describes current CPU surface temperature status detected from hardware monitor sensor. The status showed on screen will include:



4.5.8.1 CPU Warning Temperature

Select to enable or disable the hardware monitor sensor and set the warning temperature.

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
Warning Temperature	75°C /167°F	75°C /167°F	Disabled, 50/122 53/127 56/133 60°C /140°F, 63°C /145°F, 66°C /151°F, 70°C /158°F,

4.5.8.2 Current System & CPU Temperature (xx ℃/xx ℉)

The onboard hardware monitor is able to detect the temperatures of motherboard and CPU. These values refresh upon any key entry. The function is optional.

4.5.9 Current CPUFAN , CHASFAN & PWRFAN Speed

The onboard hardware monitor is able to detect chassis fan speed, CPU fan and PWR fan speed in Rotations Per Minute (RPM). These values refresh upon any key entry in the BIOS setup screen. The function is optional.

4.5.9.1 Vcore, Vcc3, +5V, +12V, -12V,-5V, VBAT & 5VSB

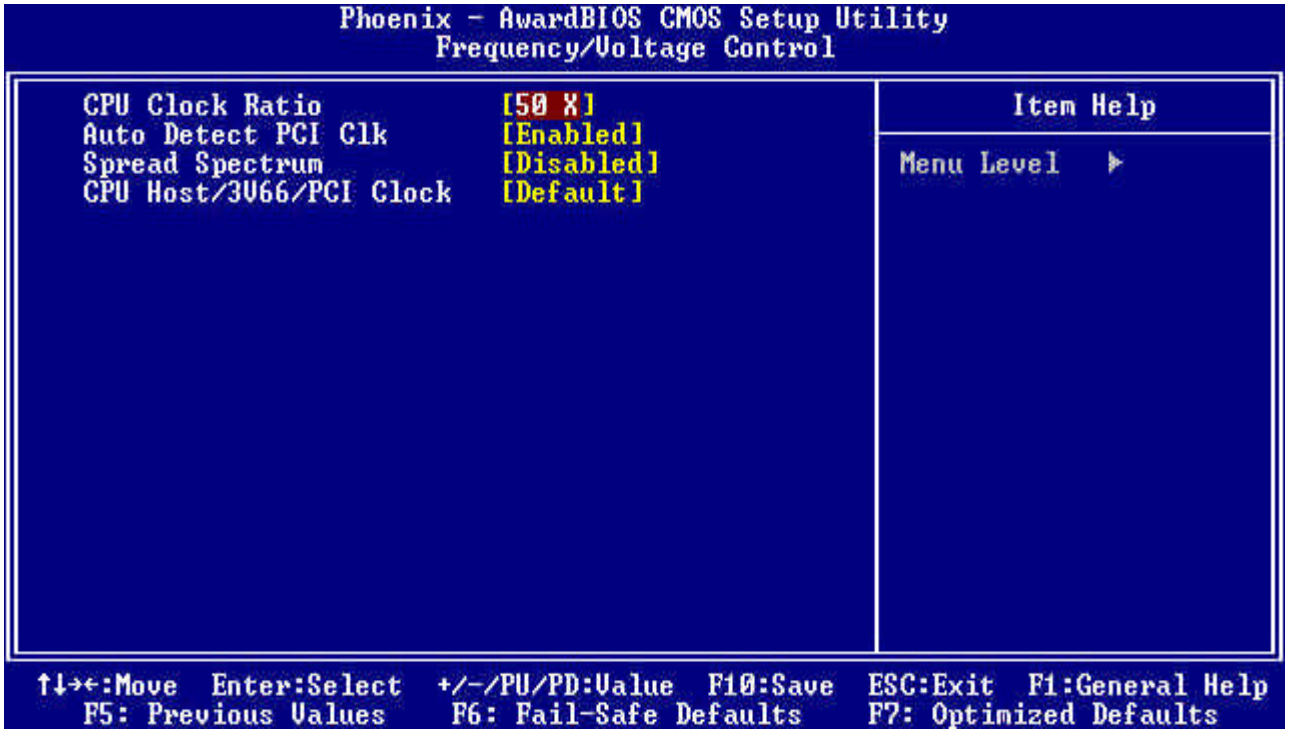
The onboard hardware monitor is able to detect the voltage output by the voltage regulators. These values refresh upon any key entry. The function is optional.

4.5.9.2 Shutdown Temperature

When you select " enable ", the CPU working temperature at over setting. Should be shutdown PC. " Disabled " is close this functions.

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
Warning Temperature	75°C /167°F	75°C /167°F	Disabled, 60°C /140°F, 65°C /145°F, 70°C /158°F, 75°C /165°F,

4.5.9.3 Frequency Control Setup Defaults



4.5.9.4 CPU Clock Ratio

The Ratio of some latest Intel Corporation fixes CPUs and VIA so the Ratio cannot be changed with the setting. If it did not fix by CPU manufacturer, it may be changed with the setting. Over specification operations are not recommended.

4.5.9.5 Auto Detect PCI CLK

If you have the EMI issue, set the option as Enabled, it keeps its interference under control.

The choice: Disable, Enable.

4.5.9.6 Spread Spectrum

Using the setting " Enabled ", for EMI testing will increase the system stability. The default setting is " Disabled ".

The choice: Disable, Enable.

4.5.9.7 CPU Host/3v66/PCI Clock

Choose Default, 100, 103, 105, 107,109,111, 114, 117,120, 127, 130 MHz for the external frequency of your CPU. You can select Default, 66, 69,70,71,73,74,76,78,80,85,87MHz. if your CPU is 100Mhz FSB and select Default, 100, 103, 105, 107,109,111,114,117, 120, 127 or 130 MHz if the CPU is 100Mhz FSB.

Warning: Over specification operations are not recommended.

The frequency-mapping table of the elements:

CPU Host/3V66	PCI
100 / 66 MHz	33 MHz
103 / 69 MHz	34 MHz
105 / 70 MHz	35 MHz
107 / 71 MHz	36 MHz
109 / 73 MHz	36 MHz
111 / 74 MHz	37 MHz
114 / 76 MHz	38 MHz
117 / 78 MHz	39 MHz
120 / 80 MHz	40 MHz
127 / 85 MHz	42 MHz
130 / 87 MHz	43 MHz

4.5.10 Load Fail-Safe Defaults

This loads the troubleshooting default values permanently stored in the ROM chips. These settings are not optimal and turn off all high performance features. You should use these values only if you have hardware problems. Highlight this option in the main menu and press <Enter>. The message below will appear.

Load Fail-Safe Defaults (Y/N)? N

If you want to process, type <Y> and press <Enter>. The default settings will be loaded.

4.5.11 Load Optimized Defaults

This feature loads optimized setting from the BIOS ROM. Use the default values as standard values for your system. Highlight this option in the main menu and press <Enter>. The message below will appear.

Load Optimized Defaults (Y/N)? N

Type <Y> and press <Enter> to load the Setup default values.

4.5.12 Set Supervisor/User Password

You can assign, modify, or cancel password settings. To modify, highlight “Set Supervisor Password” or “Set User Password” and press the <Enter> key. The screen will prompt you (“Enter Password:”). Enter your password. The maximum size of the password is 8 characters. System will prompt you to reenter the password to verify. Remember the passwords are case sensitive.

If you want to remove the passwords, either delete passwords or press <Enter> when prompting for new password.

If you want it to require password upon initial system startup and upon entering the CMOS Setup Utility, you will need to change the selection of the (Security Option) under (Advanced BIOS Features) to “System”.

If the setting is “Setup”, the system will only require the password you activate CMOS Setup Utility.

4.5.13 Save & Exit Setup

When all the changes have been made, highlight "Save & Exit Setup" and press <Enter>. The message below will appear:

Save to CMOS and Exit (Y/N)? N

Type "Y" and press <Enter>. The modifications you have made will be written into the CMOS memory, and the system will reboot.

4.5.14 Exit Without Saving

When you do not want to save the changes you have made, highlight "Exit Without Saving" and press <Enter>, the message below will appear:

Quit Without Saving (Y/N)? N

Type "Y" and press <Enter>. The system will reboot.

4.6 Flash BIOS Utility

Utilize Award Flash BIOS programming utility to update on-board BIOS for the future new BIOS version. Please contact your technical window to get this utility if necessary.

Note:

Remark or delete any installed Memory Management Utility (such as HIMEM.SYS, EMM386.EXE, QEMM.EXE, …, etc.) in the CONFIG.SYS files before running Flash-programming utility.

5. Driver Installation

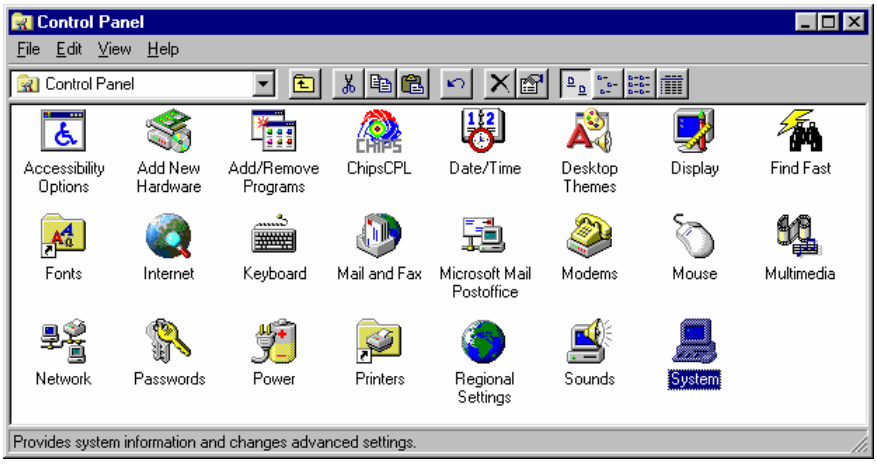
5.1 Driver Installation for Ethernet Adapter

5.1.1 Windows 9x

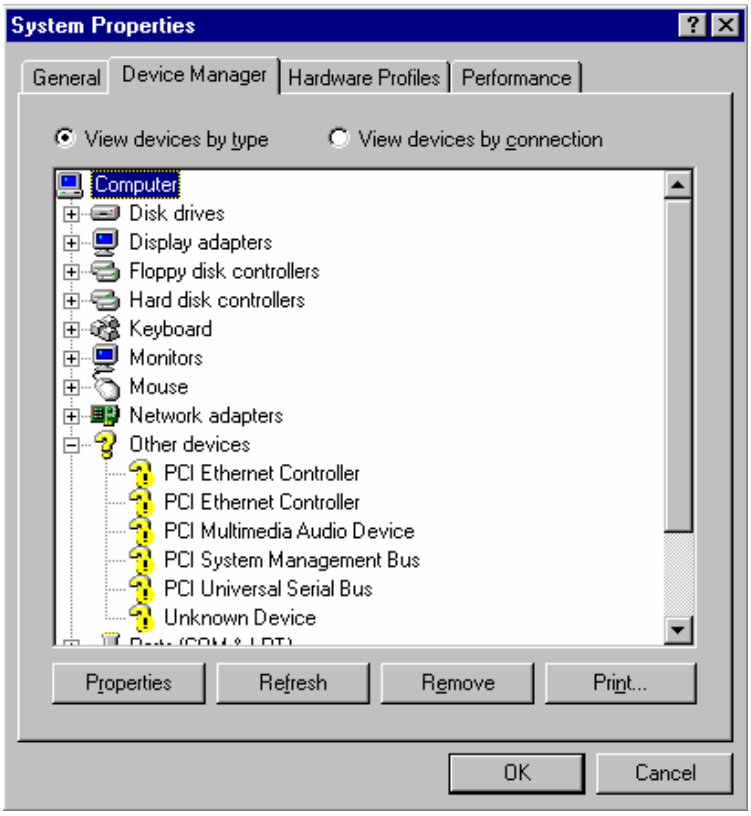
A driver for the PCI Fast Ethernet controller on board is included in the attached supporting CD-ROM. The driver for this adapter is denoted 'Realtek RTL8139C/81x PCI Fast Ethernet Adapter'.

The best way to install the driver for the Ethernet controller is to use the plug and play system of Windows 9x. The following procedures illustrate how the installation can be done.

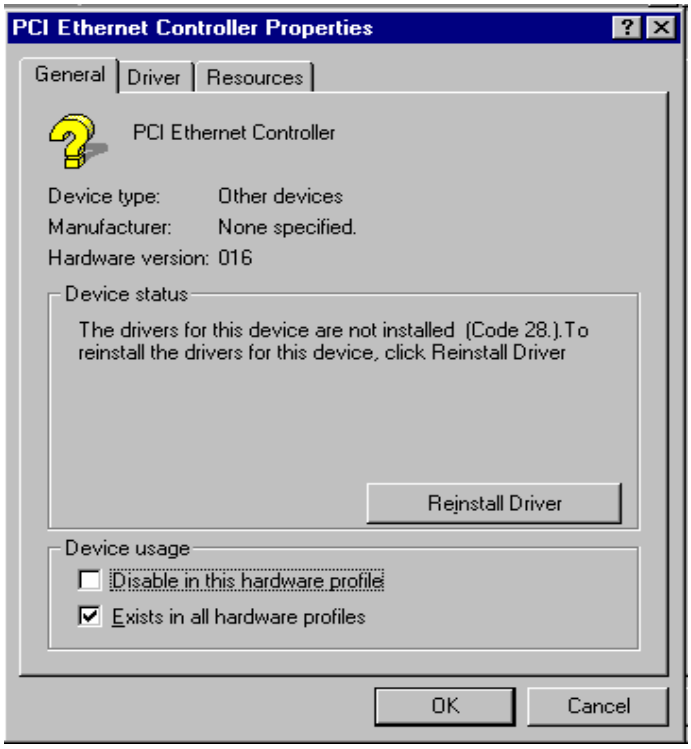
1. Start the control panel by clicking the '*Start*' button, click'*Settings*' and '*Control Panel*' from the sub-menu. Double click the 'System' icon in the control panel as shown below.



- Double click the '*System'* icon (highlighted above).
- Select the '*Device Manager'* tab.

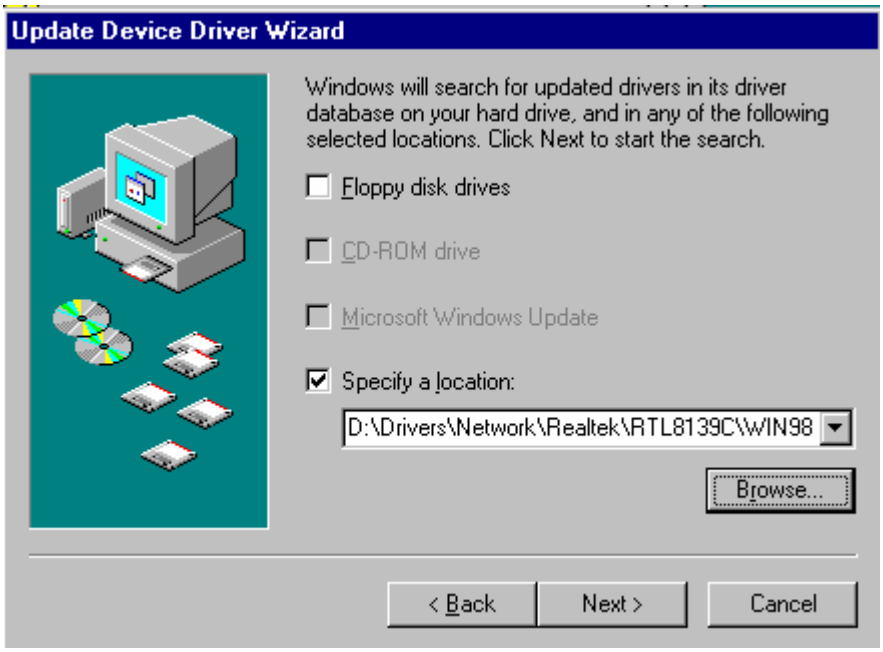


2. Double click *'PCI Ethernet Controller'*. This will show the following window. Click the '*Reinstall Driver'* button.

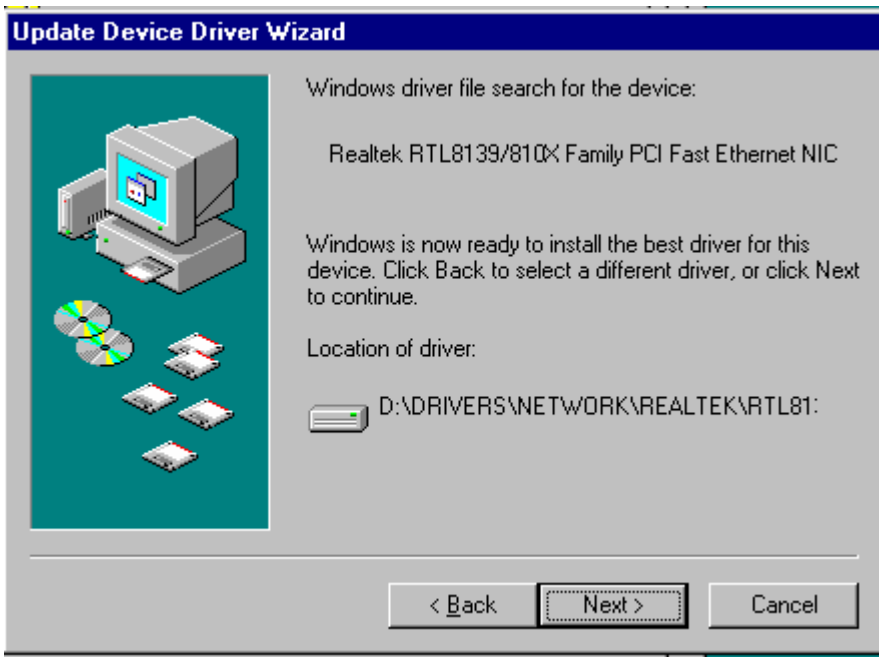


3. Click the '*Next*' button to run Add New Hardware wizard to install device driver.

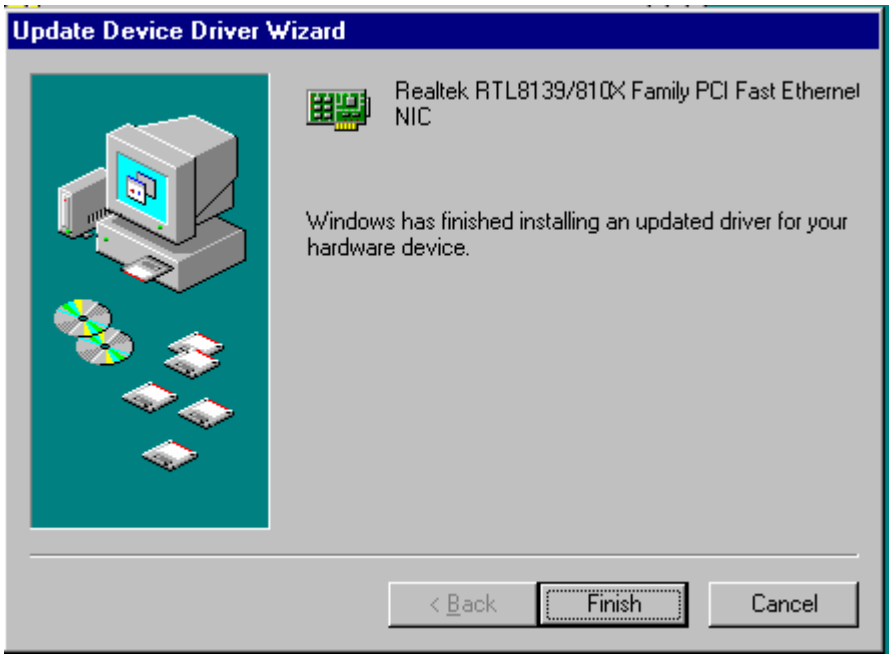
4. Specify the location of network adapter and click '*Next*' (see below).



5. Click the '*Next*' button.



6. Click the '*Finish'* button.



7. Depending on the configuration, a request for the windows disks or CD-ROM may be necessary. Insert the disk / CD-ROM and click the '*OK*' button. An entry of the directory for the files may then be required. After typing the path name, click the '*OK*' button.

8. To complete the installation, reboot the computer by clicking the '*Yes*' button in the window shown below.

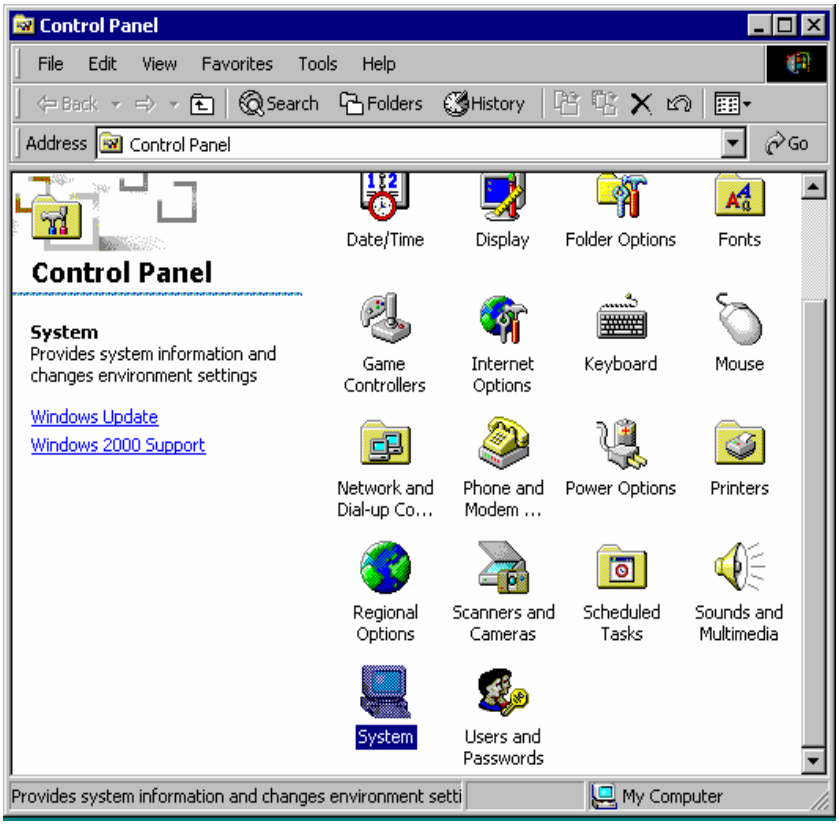
9. After the system restarts, the network adapter should be installed. Protocols, clients etc. may now be installed for the network in use.

Further configuration of the adapter may be made in the '*Advanced*' section of the driver properties. These options may be accessed through the '*Network*' icon in the control panel (Select the network adapter, click the '*Properties*' button and select the '*Advanced*' tab).

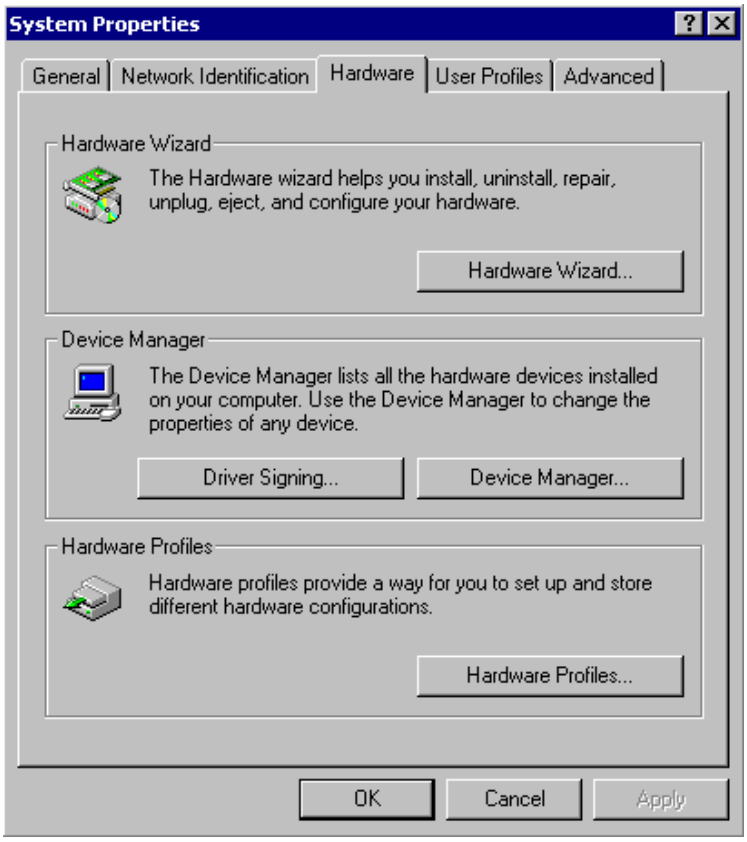
5.1.2 Windows 2000 Ethernet Installation

A driver for the PCI Fast Ethernet controller on board is included in the attached supporting CD-ROM. The driver for this adapter is denoted 'Realtek RTL8139C/81XX PCI Fast Ethernet Adapter'.

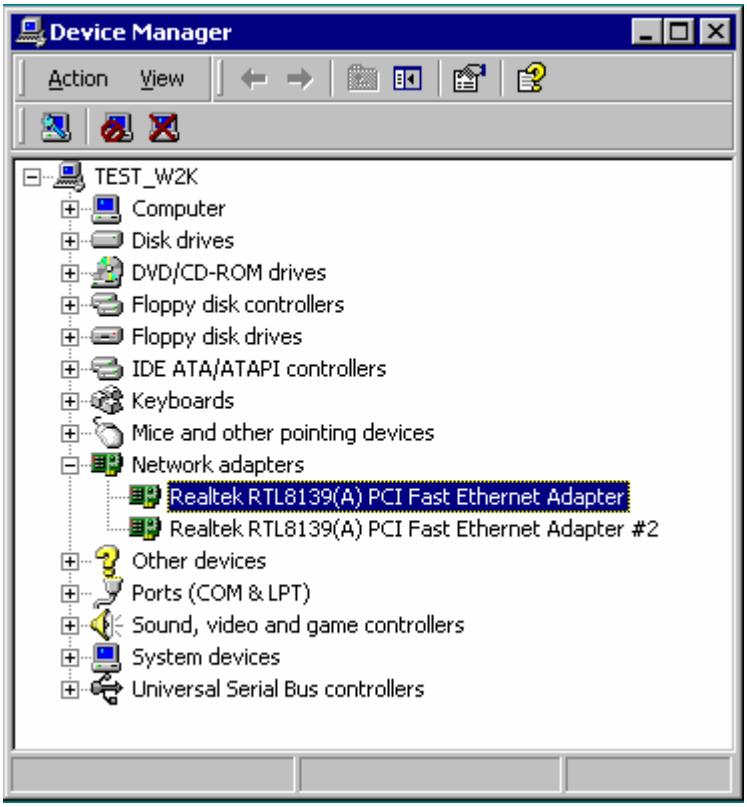
1. Start the control panel by clicking the '*Start*' button, click'*Settings*' and '*Control Panel*' from the sub-menu. Double click the 'System' icon in the control panel as shown below.



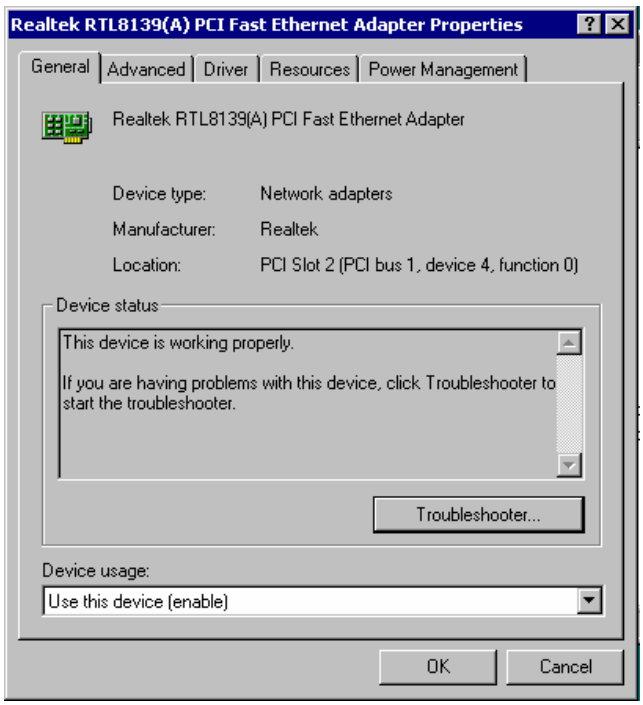
2. On the System properties window, click the *'Hardware'* tab as shown below.



3. Click the *'Device Manager…'* button to show the Device Manager.



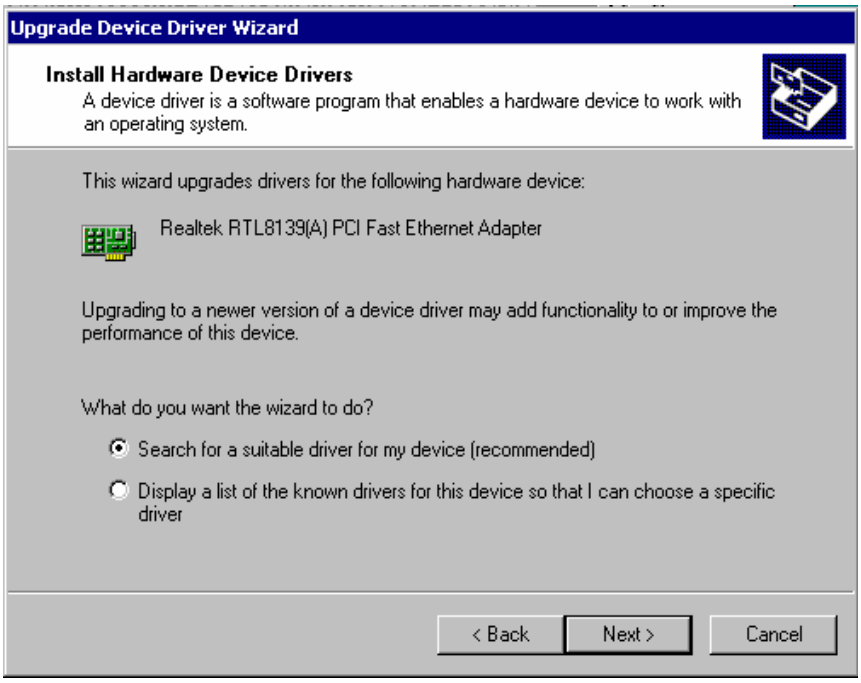
4. Double click *'Ethernet Controller' or 'Realtek RTL8139(A) PCI Fast Ethernet Adapter"*. This will show the following window. Click the '*Reinstall Driver'* button.



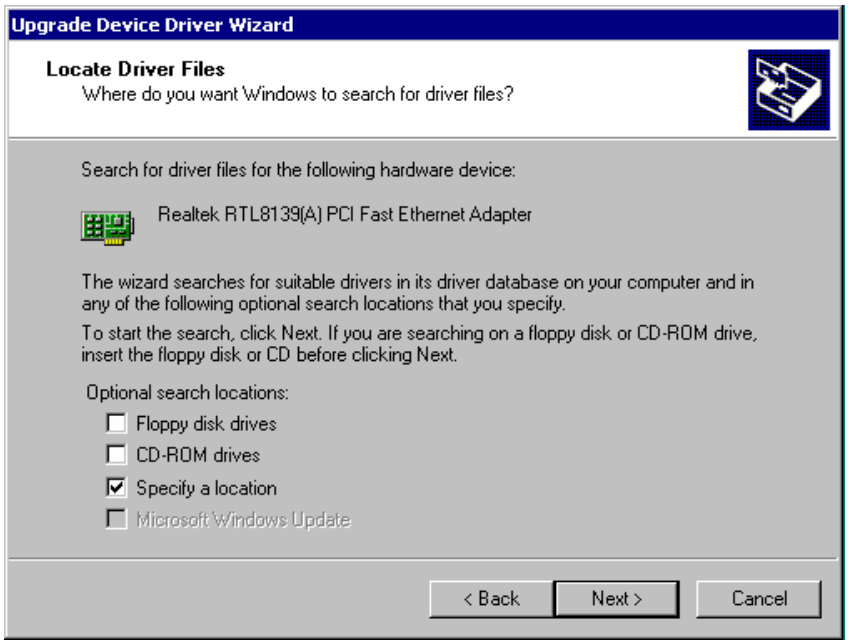
5. Click '*Driver'* tab, this will show the following window. Click the '*Update Driver..'* button.

6. Click the '*Next*' button to run upgrade device driver wizard.

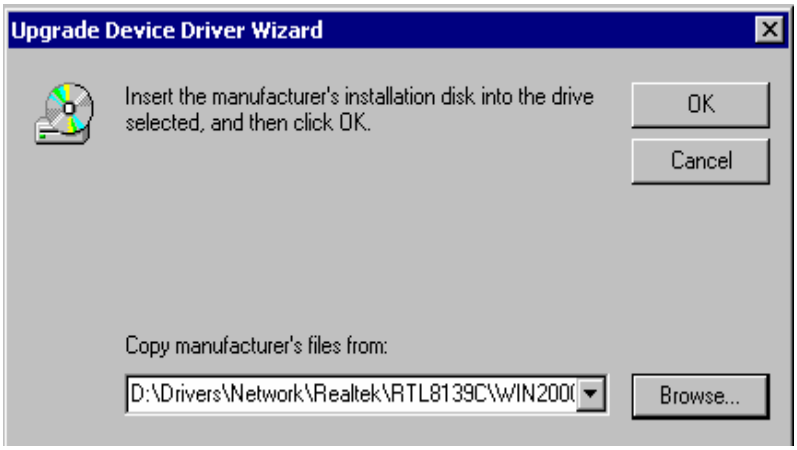
7. Click the *'Next'* button to continue the driver installation.



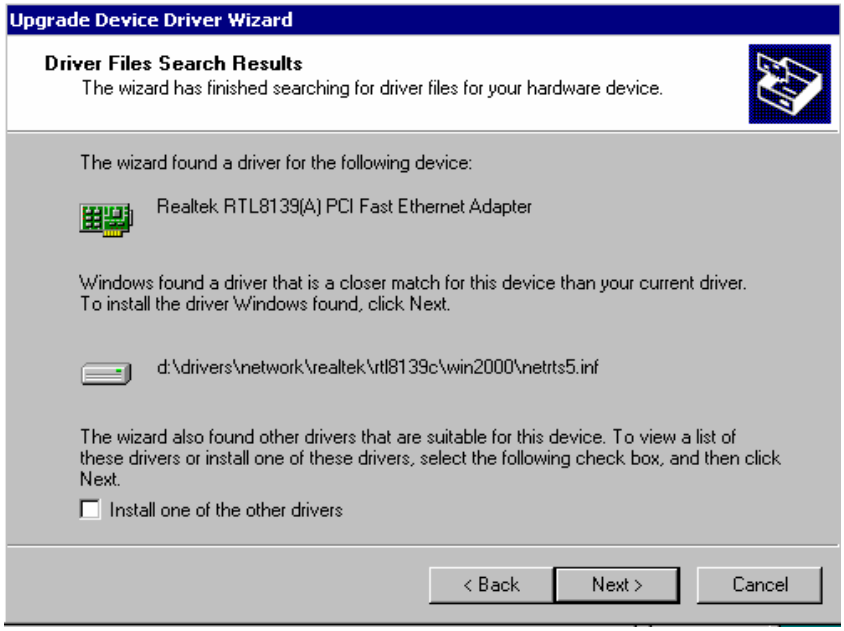
8. Select the *'Specify a location'* check item, click the *'Next'* button to continue.



9. The directory for the drivers may now be entered or click the *'Browse…'* button to select the directory. Click the *'OK'* button to continue.

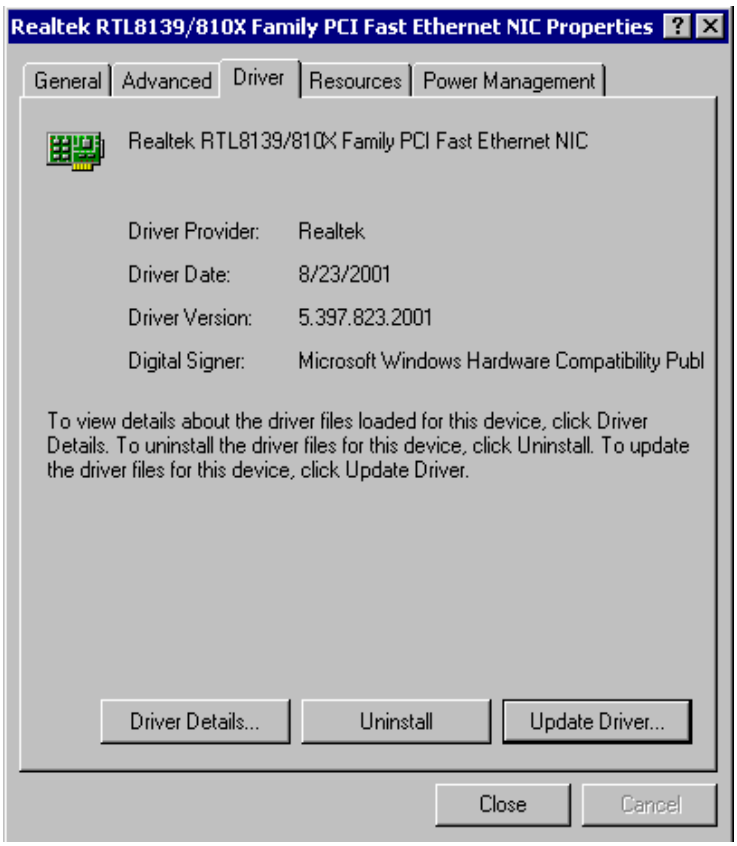


10. After system search the driver, click the *'Next'* button to continue upgrade driver.



11. After system install to drivers, the follow windows should appear, click the *'Finish'* button to finish the driver installation.

12. After finish the driver installation, system will return to Properties windows as shown below. Click the 'OK' button to return the Device Manager.

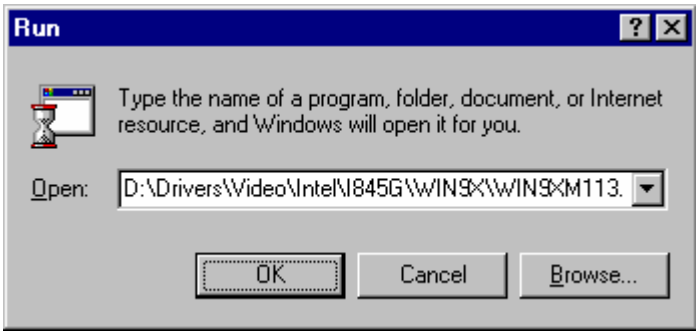


5.2 Driver Installation for Display Adapter

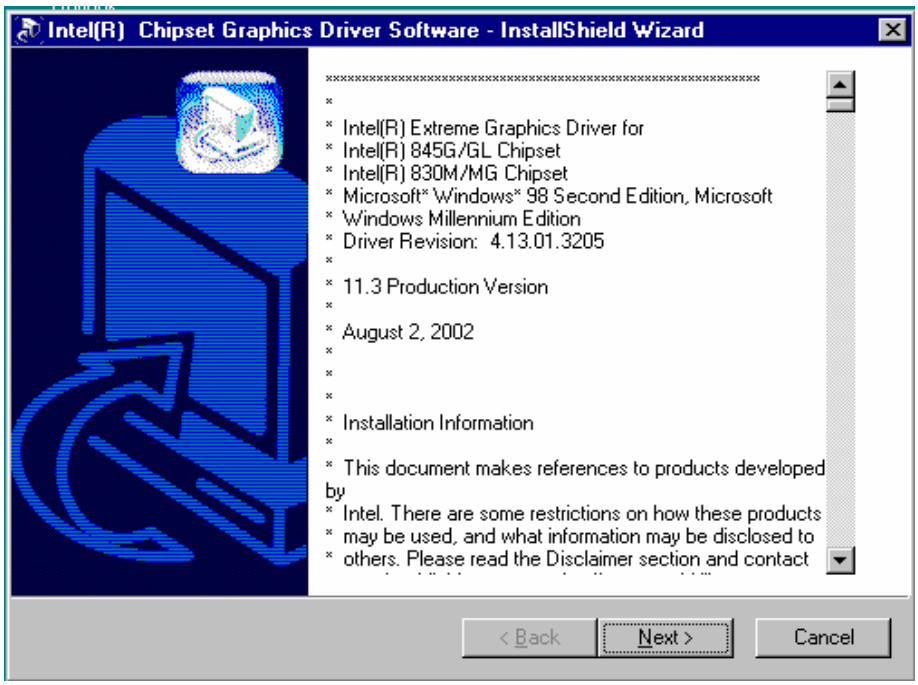
5.2.1 Windows 9x

The following steps will install the display driver for the Intel 82845GV display controller.

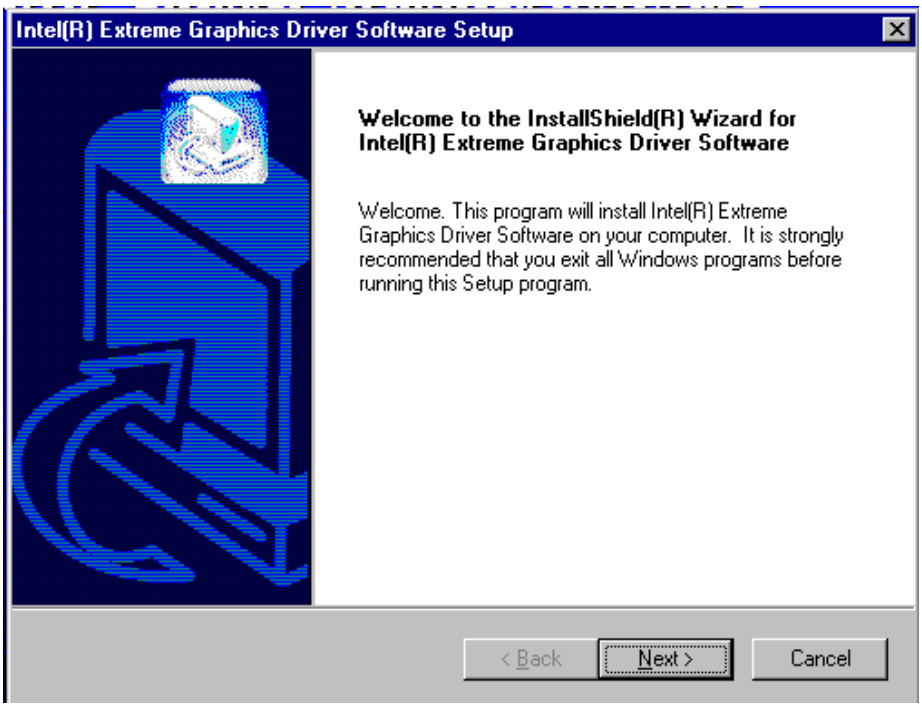
1. Click the '*Start*' button on the task bar, select '*Run*' and specify the location of Intel 82845GV Video driver setup program. This should start the driver setup program as shown below:



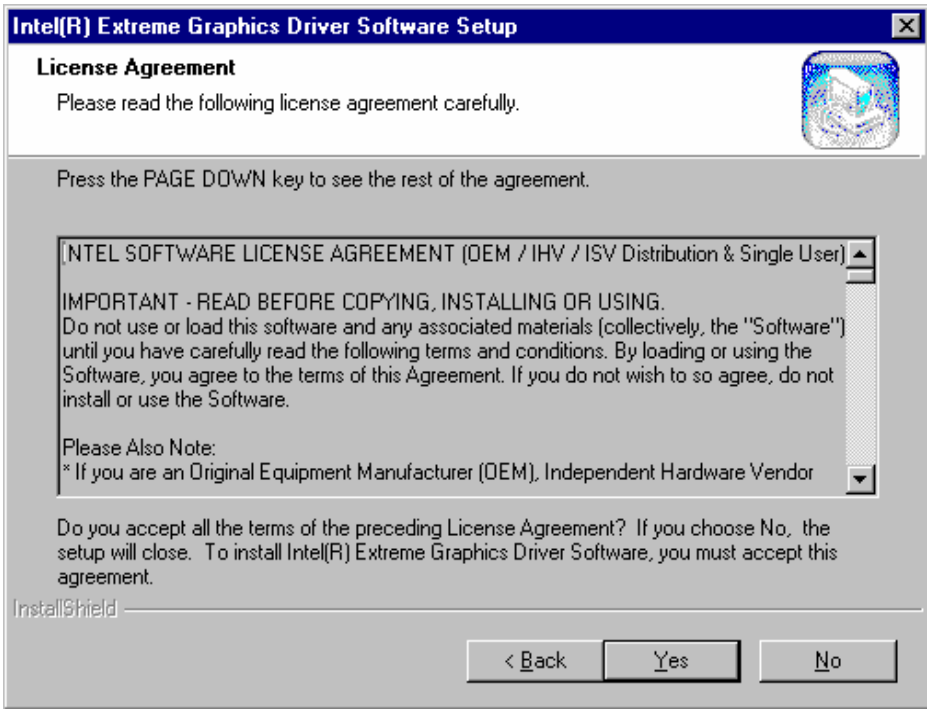
2. Click the '*Next*' as shown below.



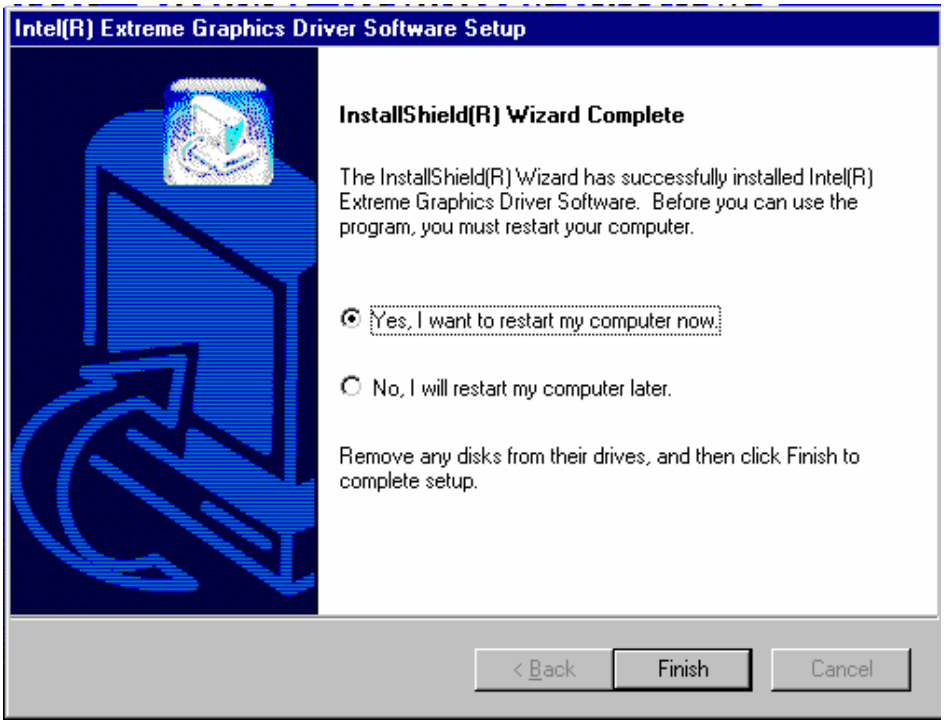
3. Click the '*Next*' as shown below.



4. Click the '*Next*' as shown below.



5. Click the '*Finish*' button to complete the driver setup.

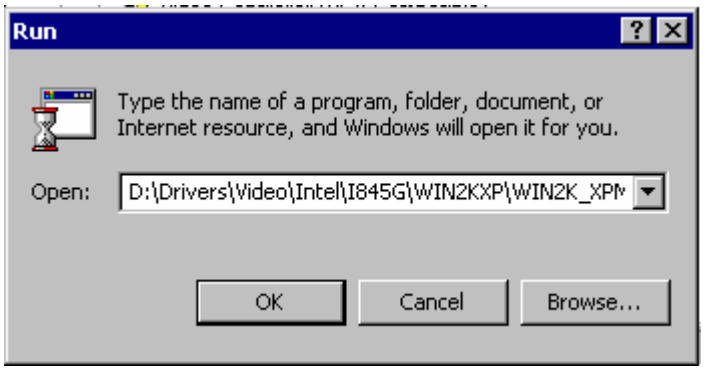


5.2.2 Windows 2000 or Windows XP Display Installation

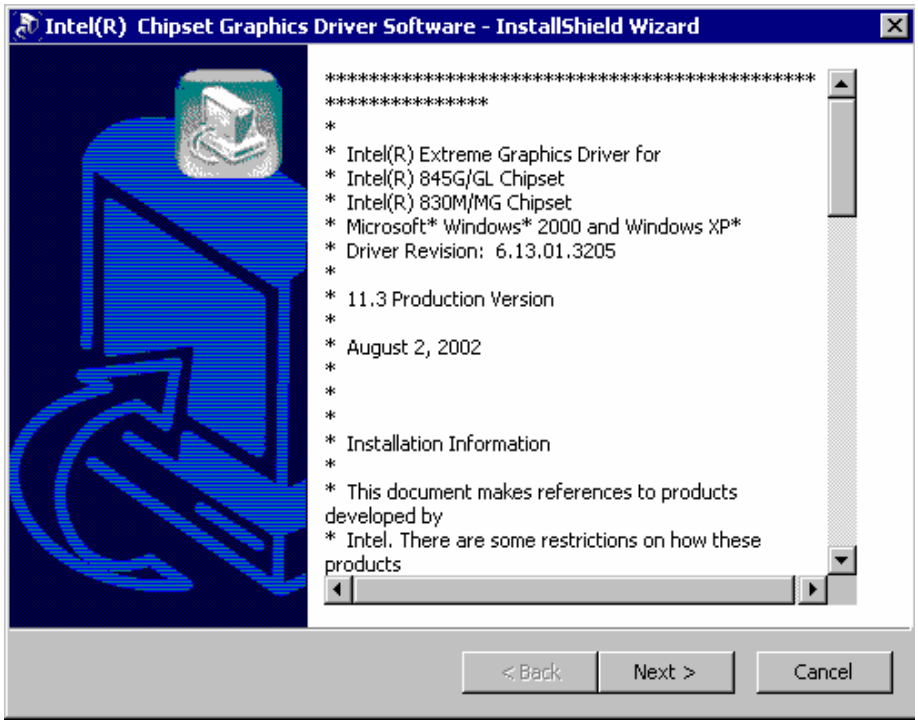
A display driver for Windows 2000 is supplied with the system on the Supporting CD-ROM.

The driver installation may be performed by following steps shown below:

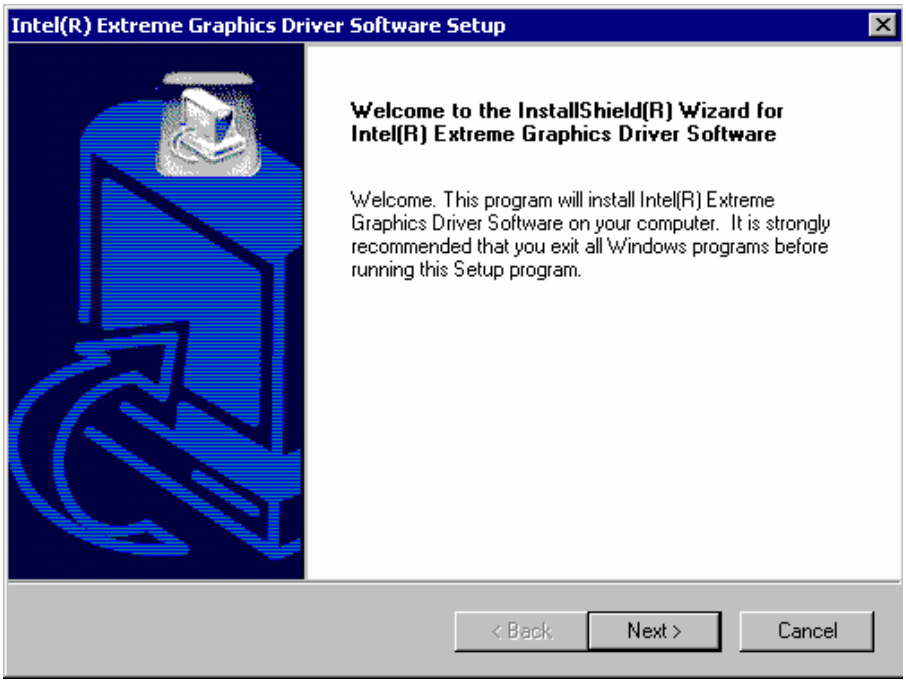
1. Click the '*Start*' button on the task bar, select '*Run*' and specify the location of Intel 82845GV Video driver setup program. This should start the driver setup program as shown below:



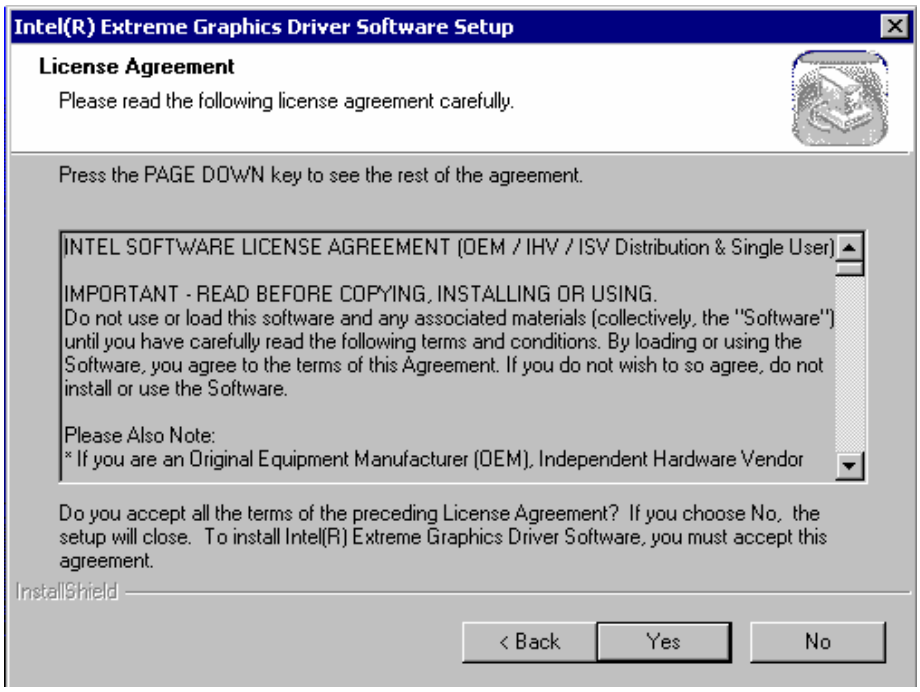
2. Click the '*Next*' as shown below.



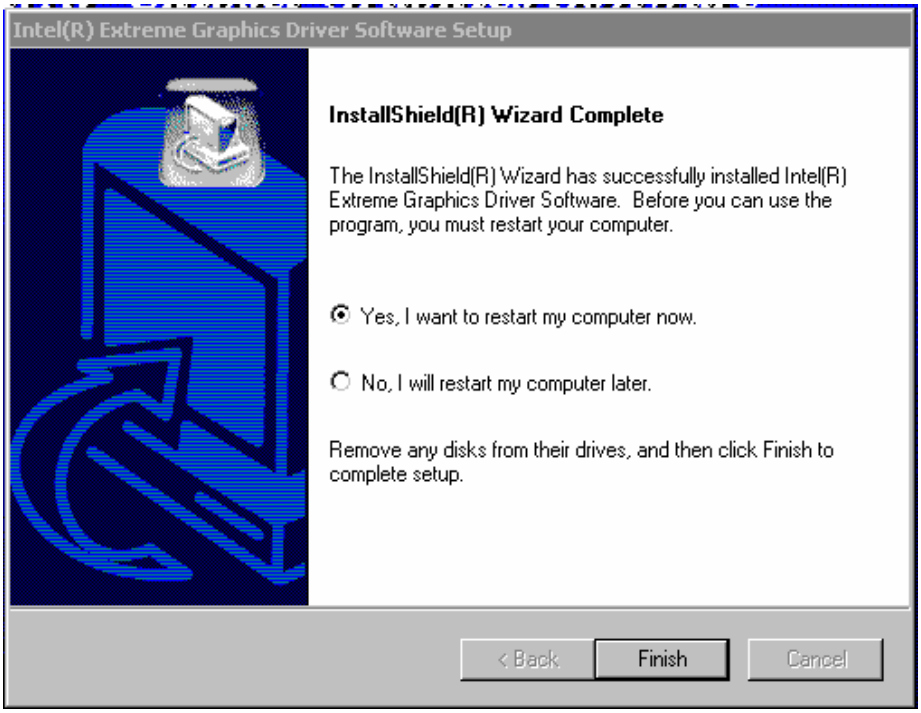
3. Click the '*Next*' as shown below.



4. Click the '*Next*' as shown below.



5. Click the '*Finish*' button to complete the driver setup.

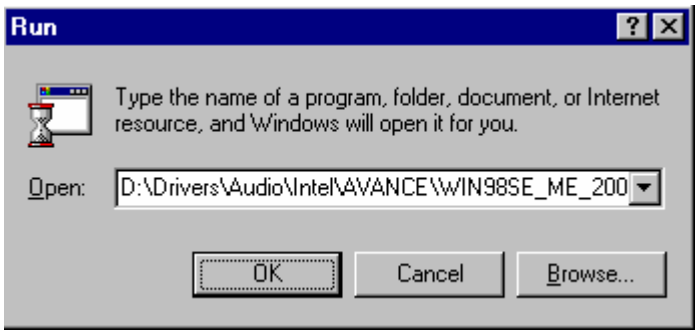


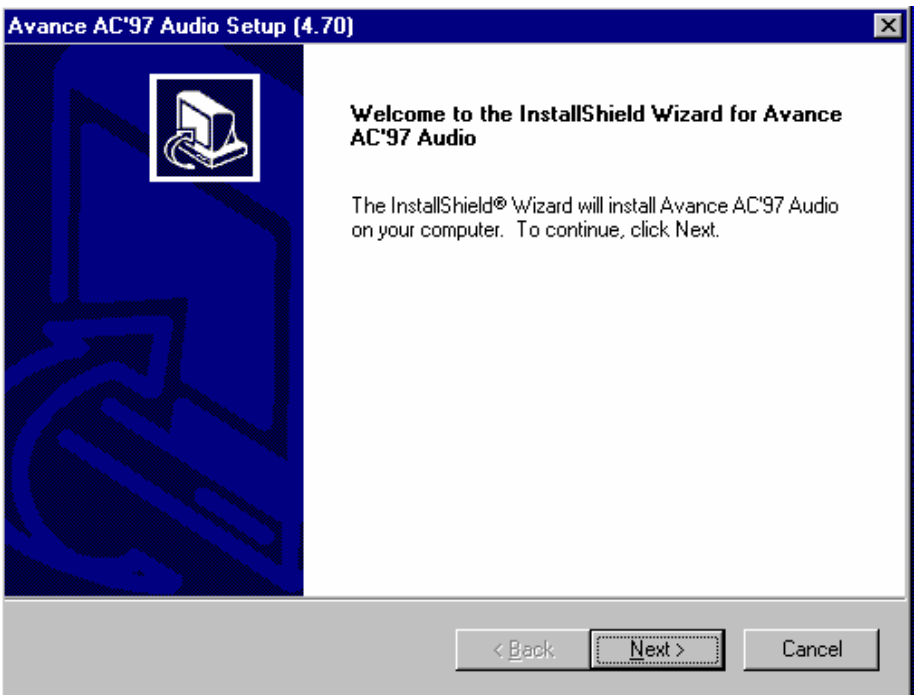
5.3 Driver Installation for Audio Adapter

5.3.1 Windows 9x, Windows 2000, Windows XP

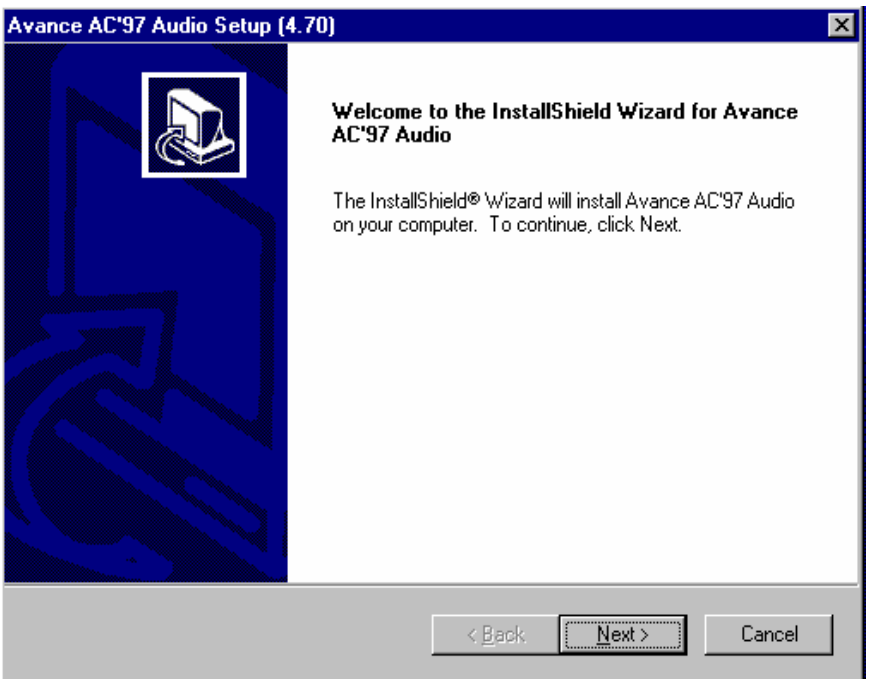
The following steps will install the audio driver for the 'Intel 82801DB AC97 Audio ' controller.

1. Click the '*Start*' button on the task bar, select '*Run*' and specify the location of Intel AC97 Audio driver setup program. This should start the Audio driver setup program as shown below:

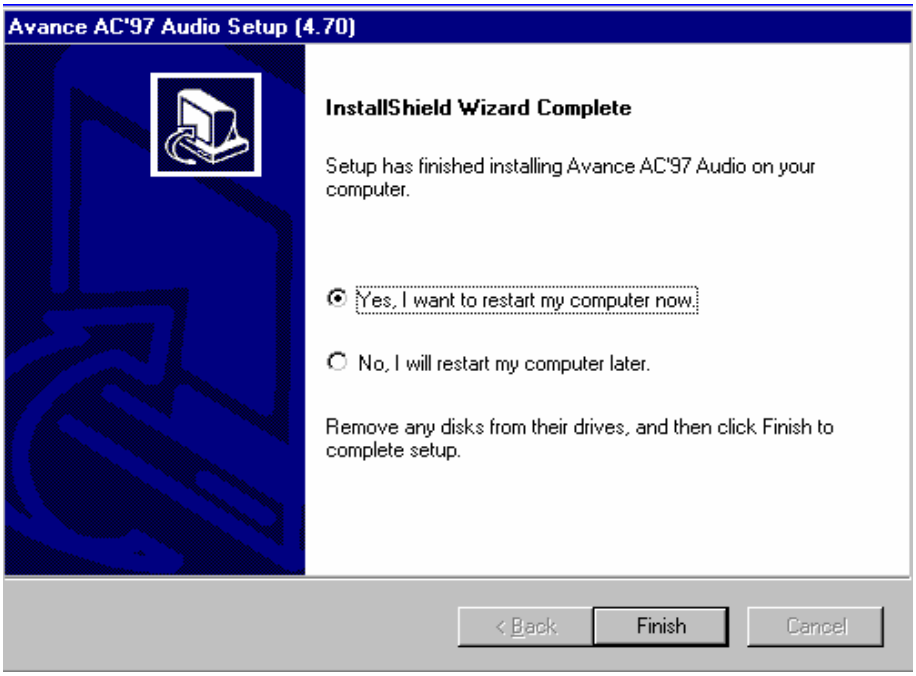




2. Select '*Next >*' as shown below.



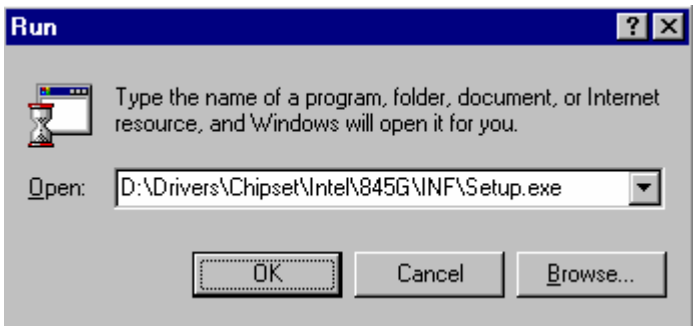
3. Click the '*Finish*' button to complete the driver setup.



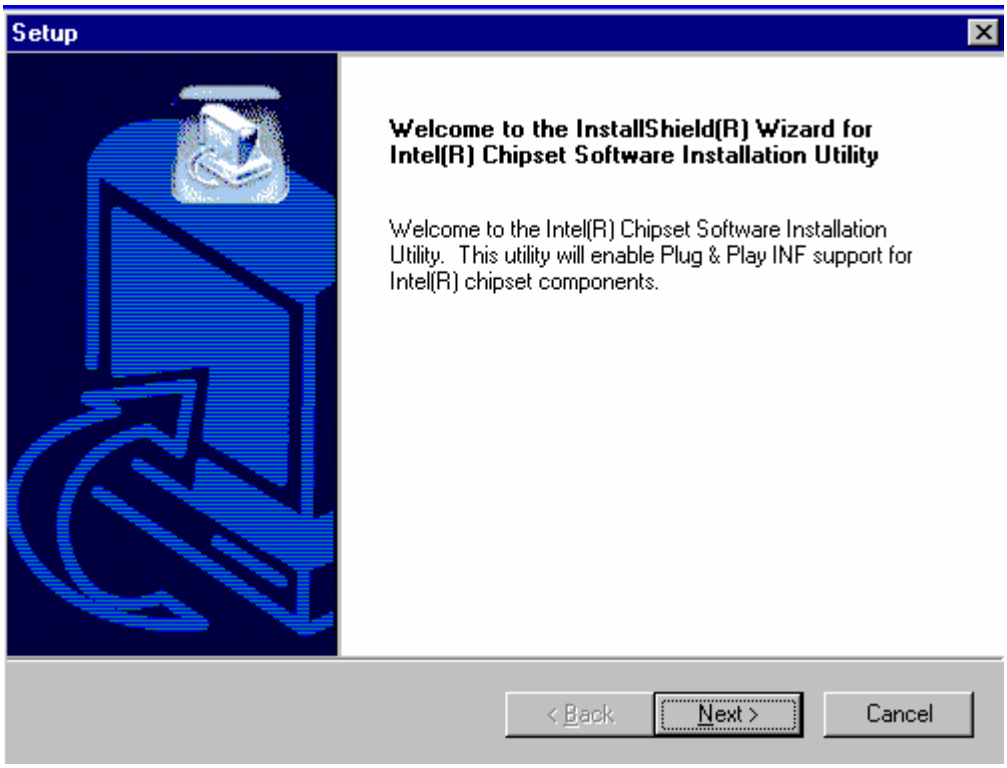
5.4 Driver Installation for Intel 845 Chipset

The following steps show how to install the Intel 82845G chipset driver.

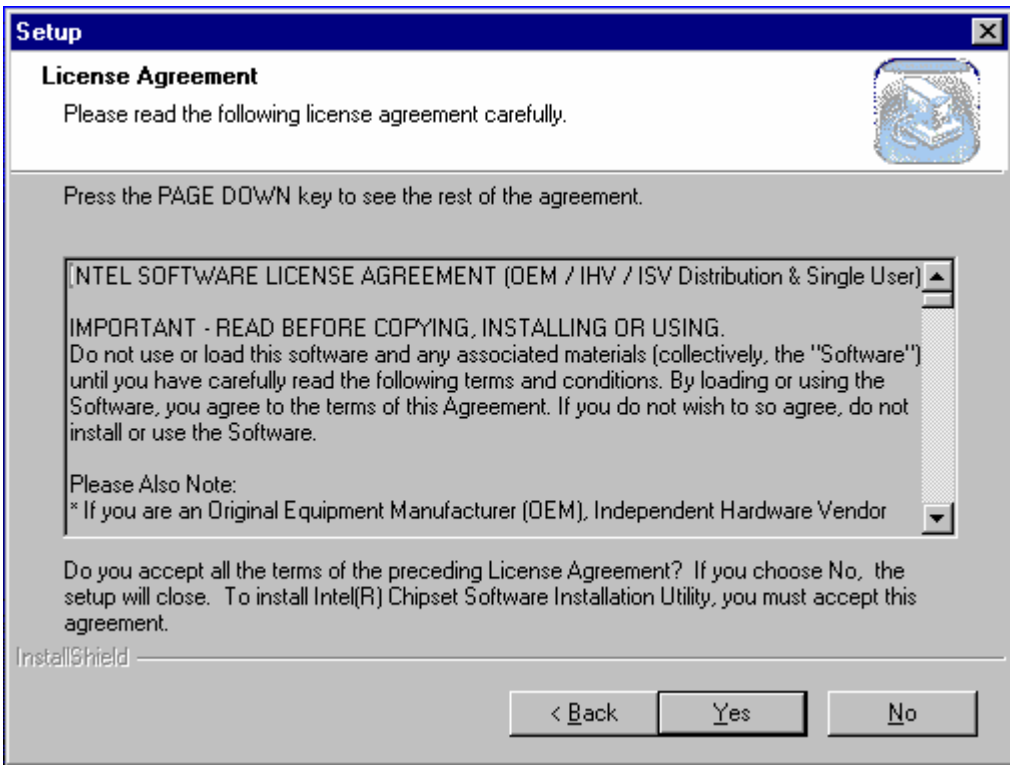
1. Click the '*Start*' button on the task bar, select '*Run*' and specify the location of Intel 82845G chipset driver setup program. This should start the Intel Chipset driver setup program as shown below:



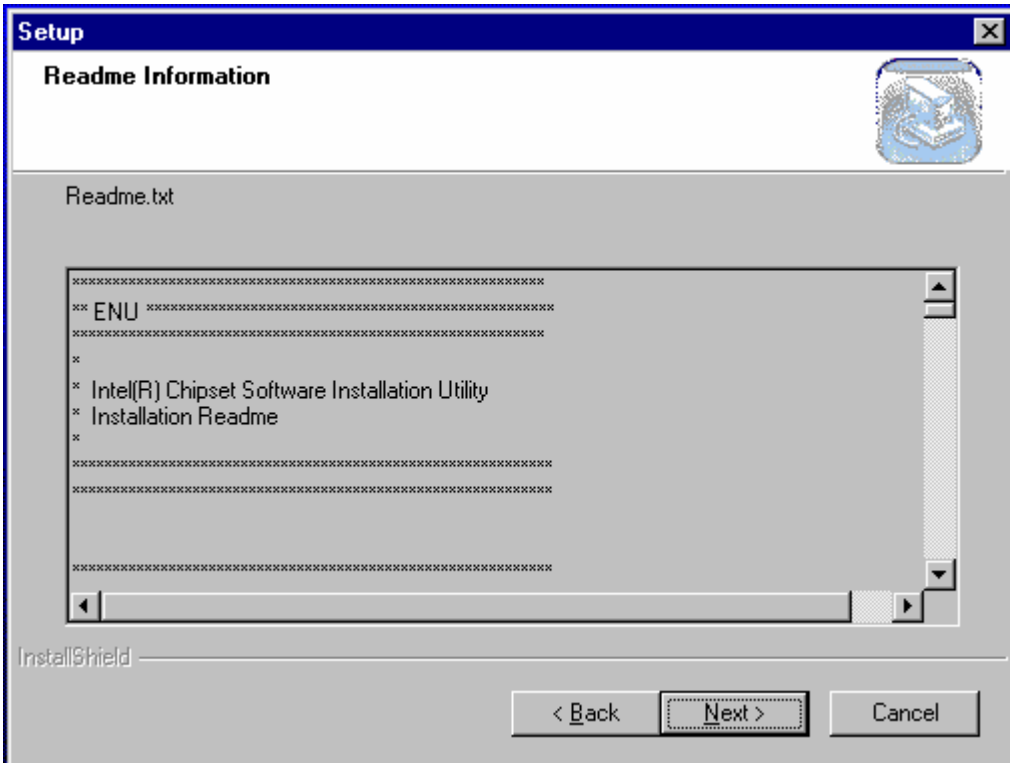
2. Press '*Next*' to continue installation.



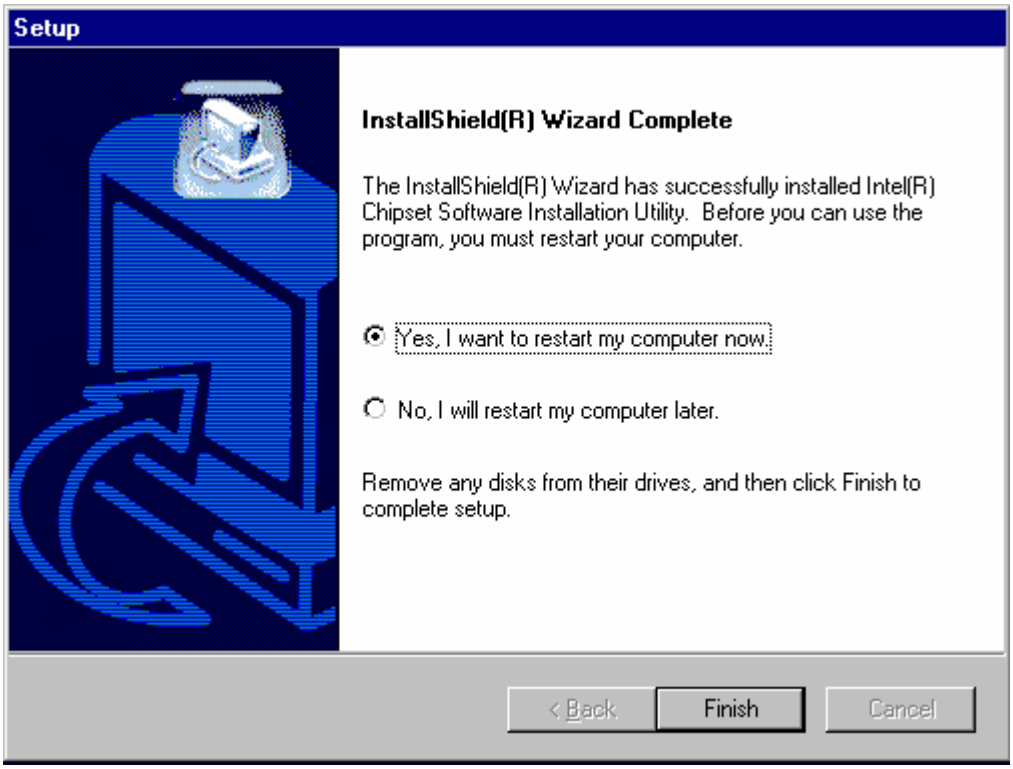
3. Press '*Next*' to continue installation.



4. Press '*Next*' to continue installation.



5. Click the '*Finish*' button to complete the driver setup.



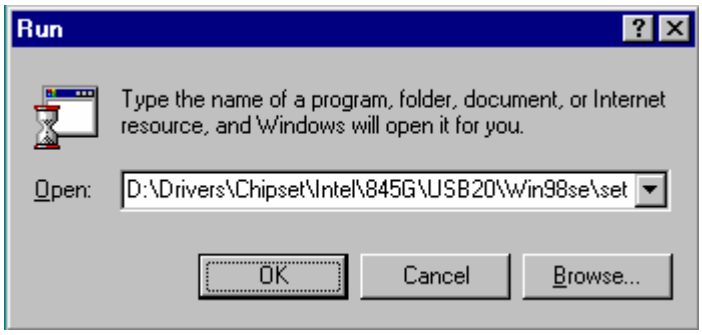
6. To complete the driver installation and start the driver services, please reboot the computer.

5.5 Driver Installation for Intel 845G USB2.0

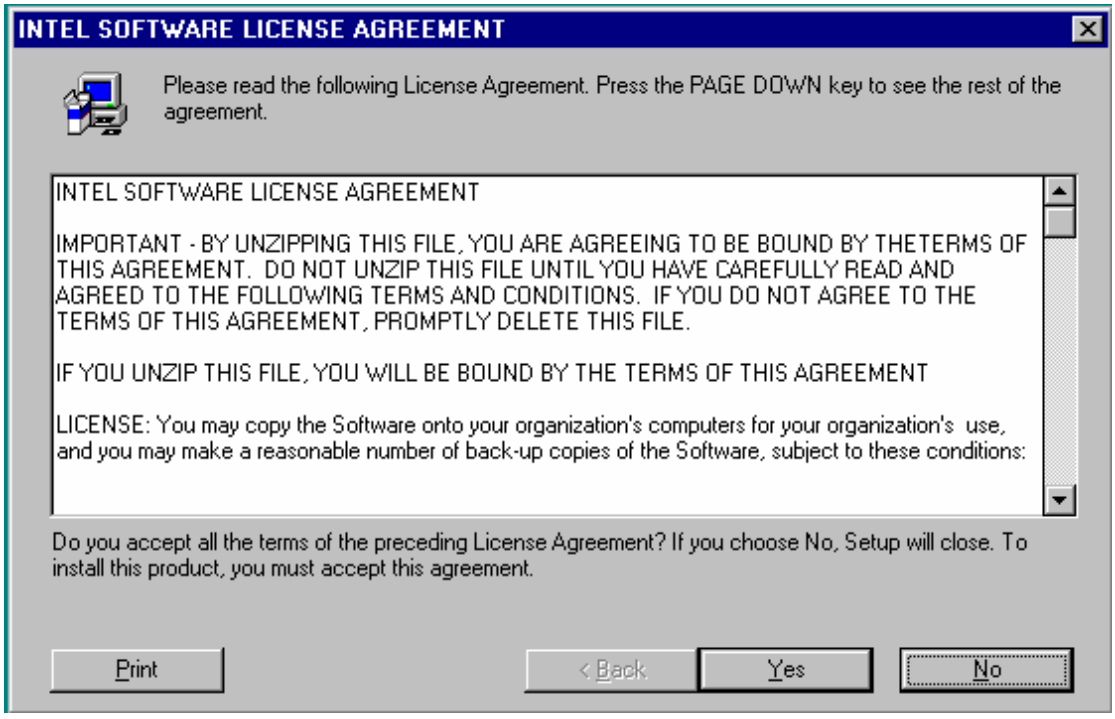
5.5.1 Windows 9x

The following steps show how to install the Intel 82845G USB2.0 driver.

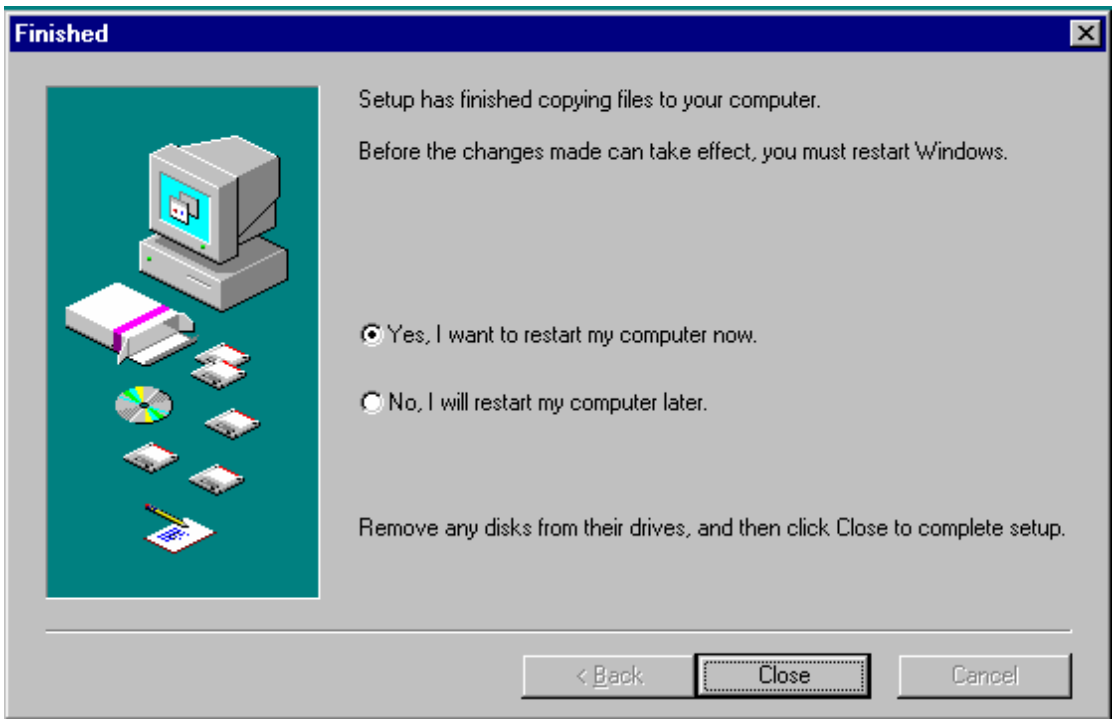
1. Click the '*Start*' button on the task bar, select '*Run*' and specify the location of Intel 82845G chipset driver setup program. This should start the Intel Chipset driver setup program as shown below:



2. Press '*Yes*' to continue installation.



3. Press '*Close*' to Finish installation.



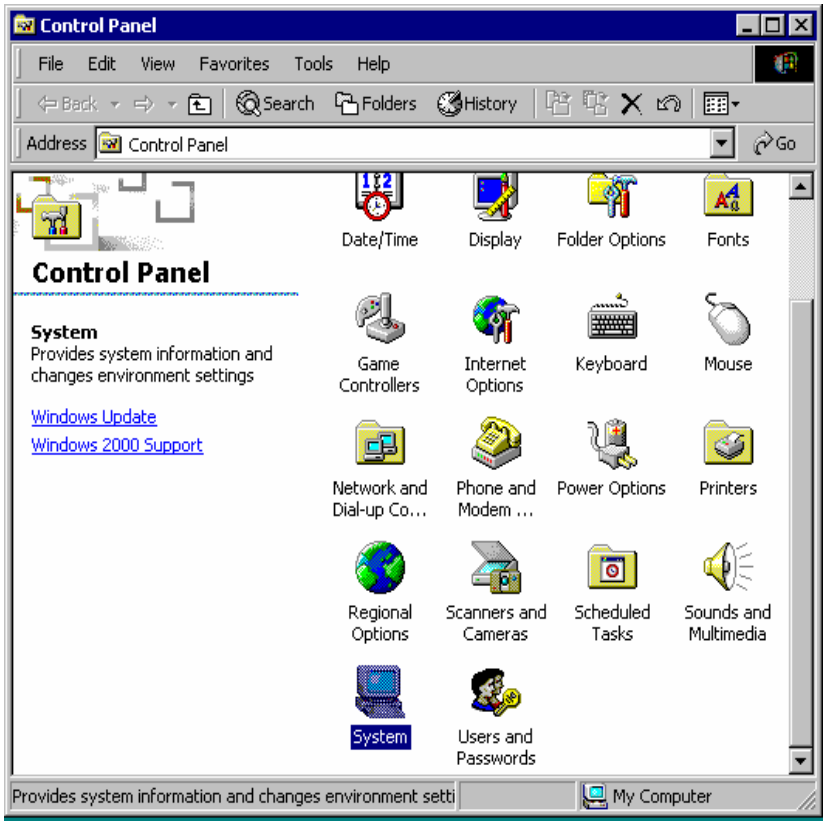
7. To complete the driver installation and start the driver services, please reboot the computer.

5.5.2 Windows 2000 USB 2.0 Installation

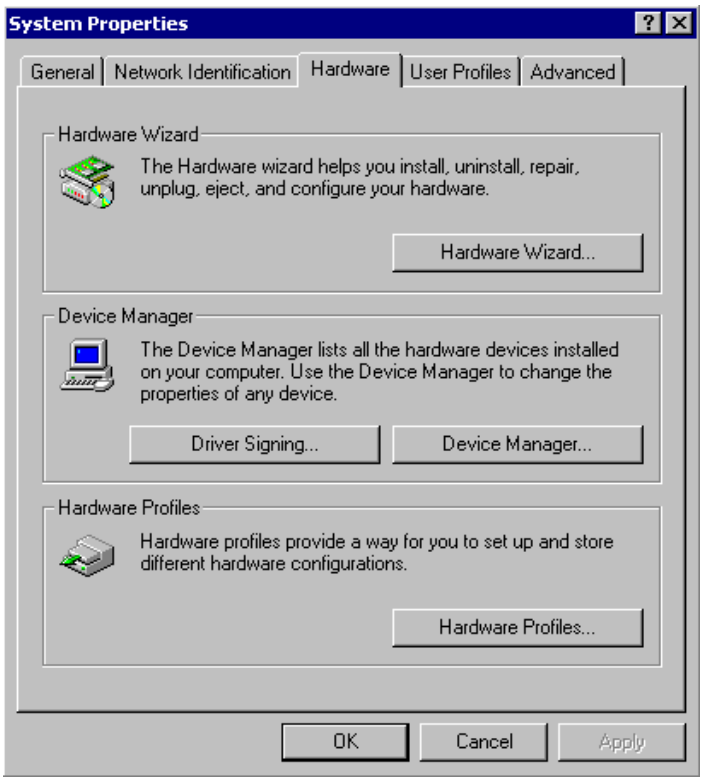
An USB 2.0 driver for Windows 2000 is supplied with the system on the supporting CD-ROM.

The driver installation may be performed by the following steps:

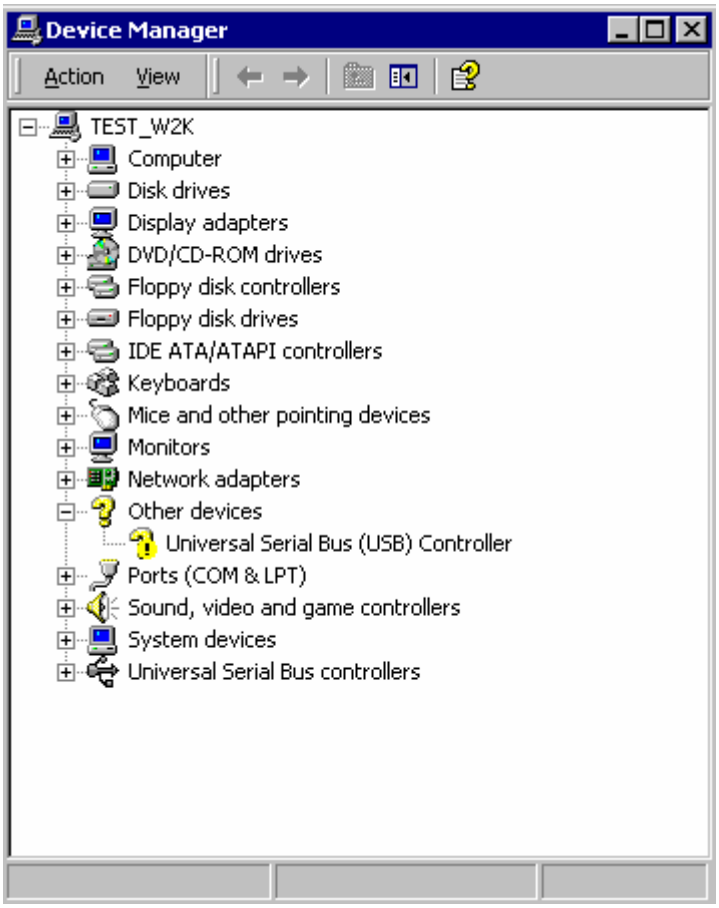
1. Start the control panel by clicking the '*Start*' button, click'*Settings*' and '*Control Panel*' from the sub-menu. Double click the 'System' icon in the control panel as shown below.



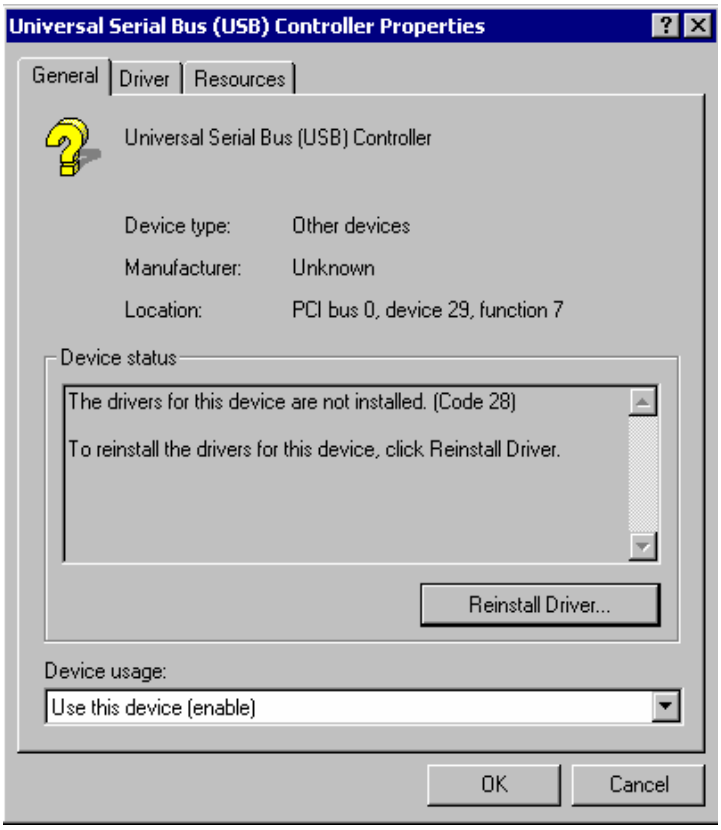
2. On the System properties window, click the 'Hardware' tab as shown below.



3. Click the '*Device Manager…*' button to show the Device Manager.



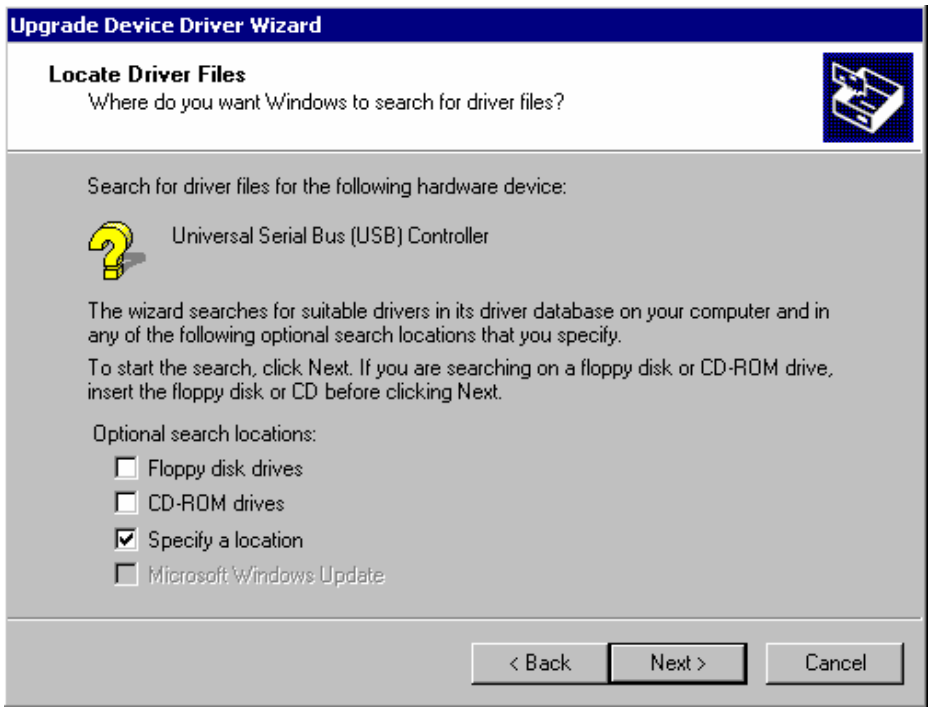
4. Double click *'Universal Serial Bus(USB) Controller'*. This will show the following window. Click the '*Reinstall Driver'* button.



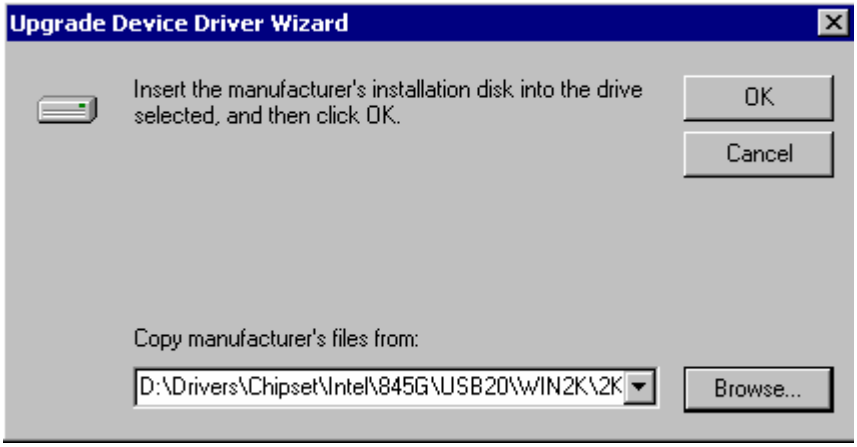
5. Click the '*Next*' button to run upgrade device driver wizard.

6. Click the *'Next'* button to continue the driver installation.

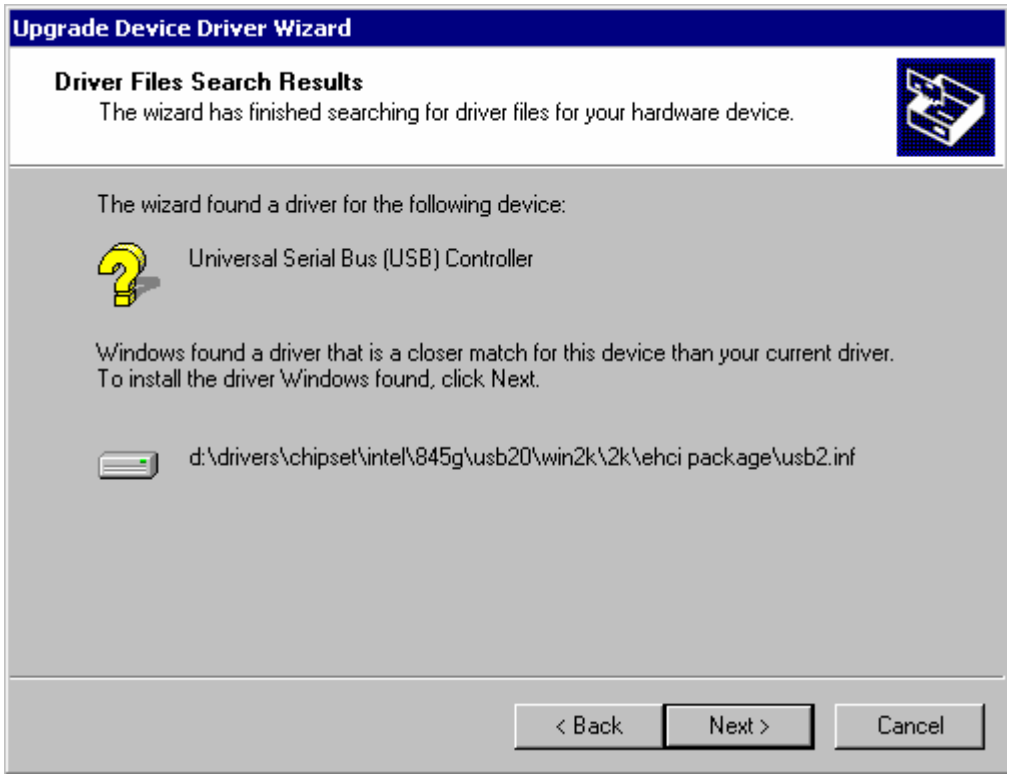
7. Select the *'Specify a location'* check item, click the *'Next'* button to continue.



8. The directory for the drivers may now be entered or click the *'Browse…'* button to select the directory. Click the *'OK'* button to continue.

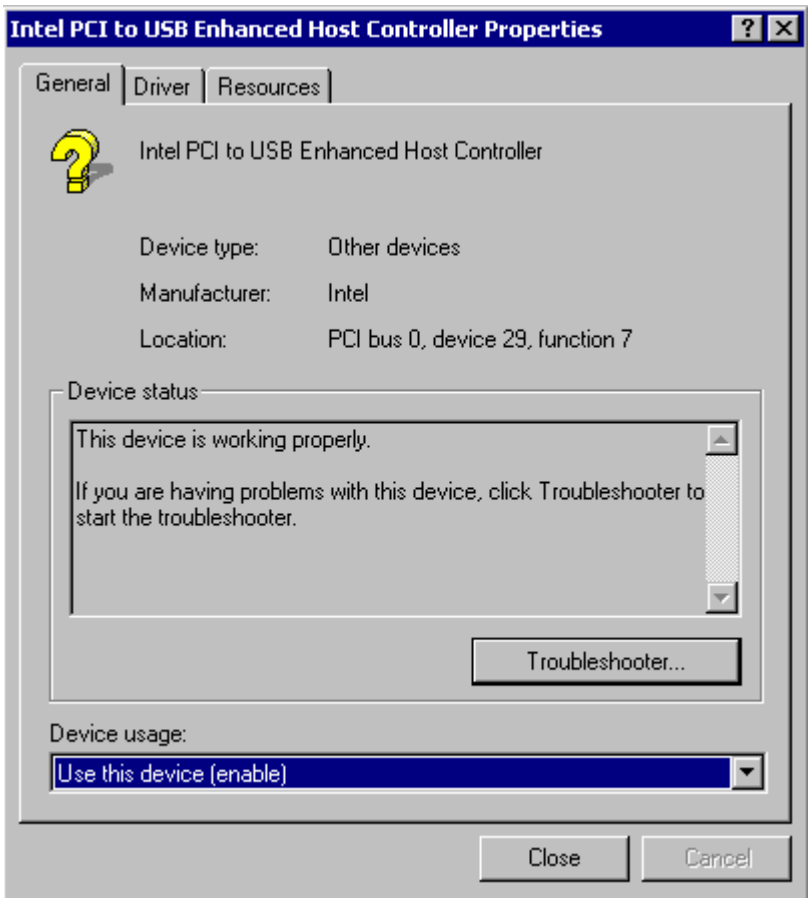


9. After system search the driver, click the *'Next'* button to continue upgrade driver.

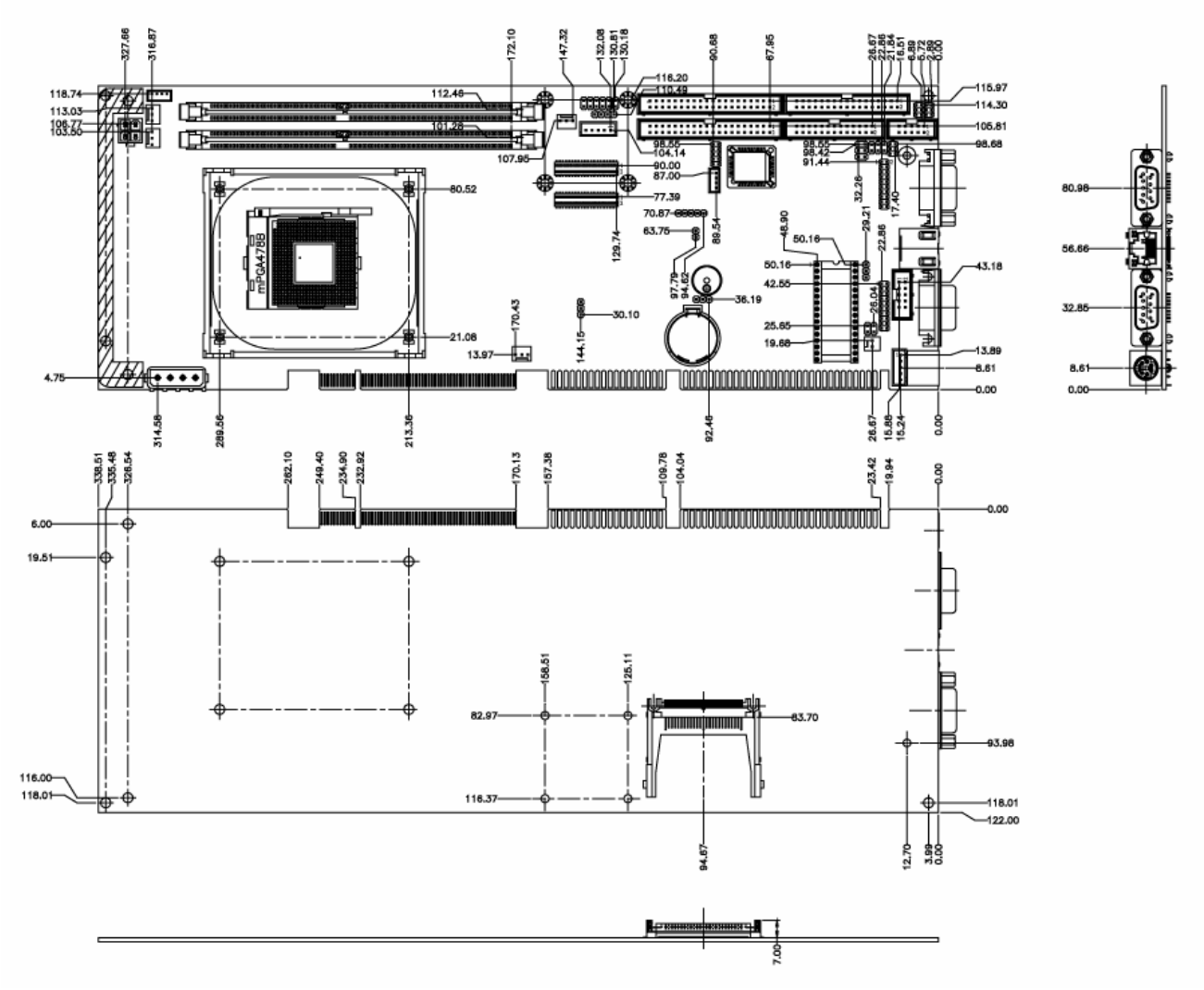


10. After system install to drivers, the follow windows should appear, click the *'Finish'* button to finish the driver installation.

11. System will show the driver information as shown below



6. Measurement Drawing



Appendix A: BIOS Revisions

BIOS Rev.

New Features

Bugs/Problems Solved

Known Problems

Appendix B: System Resources

Memory Map

The following table indicates memory map of ECB-875. The address ranges specify the runtime code length.

Address Range	Description	Note
00000000h-0009FFFFh	System board	
0009F000h-000BFFFFh	PCI bus	
000A0000h-000BFFFFh	Intel (R) 82845G Graphics Controller	
000CB200h-000DFFFFh	PCI bus	
000CB200h-000CBFFFh	Motherboard resources	
000F0000h-000F3FFFh	Motherboard resources	
000F4000h-000F7FFFh	Motherboard resources	
000F8000h-000FFFFFh	Motherboard resources	
00100000h-00FFFFFFh	System board	
3F800000h-FEBFFFFFh	PCI bus	
E0000000h-E7FFFFFFh	Intel (R) 82845G Graphics Controller	
EC000000h-EC0000FFh	Realtek RTL8139 Family PI Fast Ethernet NIC #2	
EC001000h-EC0010FFh	Realtek RTL8139 Family PI Fast Ethernet NIC	
EC100000h-EC17FFFFh	Intel (R) 82845G Graphics Controller	
EC180000h-EC1803FFh	Intel (R) PCI to USB Enhanced Host Controller	
EC181000h-EC1811FFh	Realtek AC'97 Audio	
EC182000h-EC1820FFh	Realtek AC'97 Audio	
FEBFFC00h-FEBFFFFFh	Intel (R) 82801DB Ultra ATA Storage Controller - 24 CB	
FEC00000h-FEC0FFFFh	System board	
FEE00000h-FEE0FFFFh	System board	
FFB00000h-FFB7FFFFh	System board	
FFB80000h-FFBFFFFFh	Intel (R) 82802 Firmware Hub Device	
FFF00000h-FFFFFFFFh	System board	

I/O – Map

Certain I/O addresses are subject to change during boot as PnP managers may relocate devices or functions. The addresses shown in the table are typical locations.

I/O Port	Description	Note
00000000-0000000F	Direct memory access controller	
00000010-0000001F	PCI bus	
00000020-00000021	Programmable interrupt controller	
00000022-0000003F	PCI bus	
00000040-00000043	System timer	
00000044-00000047	PCI bus	
0000004C-0000006F	PCI bus	
00000060-00000060	PC/AT Enhanced PS/2 Keyboard (101/102 – Key)	
00000061-00000061	System speaker	
00000064-00000064	PC/AT Enhanced PS/2 Keyboard (101/102 – Key)	
00000070-00000071	System CMOS/real time clock	
00000072-0000007F	PCI bus	
00000081-00000083	Direct memory access controller	
00000087-00000087	Programmable interrupt controller	
00000089-0000008B	Direct memory access controller	
0000008F-00000091	Direct memory access controller	
00000090-00000091	PCI bus	
00000093-0000009F	PCI bus	
000000A0-000000A1	Programmable interrupt controller	
000000A2-000000BF	PCI bus	
000000C0-000000DF	Direct memory access controller	
000000D0-000000EF	PCI bus	
000000F0-000000FF	Numeric data processor	
00000100-00000CF7	PCI bus	
00000170-00000177	Secondary IDE Channel	
000001F0-000001F7	Primary IDE Channel	
00000200-00000200	Standard Game Port	
00000201-00000207	Standard Game Port	
00000274-00000277	ISAPNP Read Data Port	
00000279-00000279	ISAPNP Read Data Port	
000002F8-000002FF	Communications Port (COM2)	
00000330-00000331	MPU-401 Compatible MIDI Device	
00000376-00000376	Secondary IDE Channel	
00000378-0000037F	Printer Port (LPT1)	
000003B0-000003BB	Intel ® 82845G Graphics Controller	
000003C0-000003DF	Intel ® 82845G Graphics Controller	
000003F0-000003F5	Standard floppy disk controller	

I/O Port	Description	Note
000003F6-000003F6	Primary IDE Channel	
000003F7-000003F7	Standard floppy disk controller	
000003F8-000003FF	Communications Port (COM1)	
00000500-0000051F	Intel ® 82801DB/DBM SMBus Controller – 24C3	
00000778-0000077B	Printer Port (LPT1)	
00000A79-00000A79	ISAPNP Read Data Port	
00000D00-0000FFFF	PCI bus	
0000C000-0000C0FF	Realtek RTL8139 Family PCI Fast Ethernet NIC #2	
0000C400-0000C4FF	Realtek RTL8139 Family PCI Fast Ethernet NIC	
0000D000-0000D01F	Intel ® 82801DB/DBM USB Universal Host Controller – 24C4	
0000D400-0000D41F	Intel ® 82801DB/DBM USB Universal Host Controller – 24C7	
0000D800-0000D81F	Intel ® 82801DB/DBM USB Universal Host Controller – 24C2	
0000E000-0000E0FF	Realtek AC'97 Audio	
0000E400-0000E43F	Realtek AC'97 Audio	
0000F000-0000F00F	Intel ® 82801DB Ultra ATA Storage Controller – 24CB	

Interrupt Usage.

The actual interrupt settings depend on the PnP handler, the table below indicates the typical settings.

Interrupt	Description	Note
ISA 0	System timer	
ISA 1	PC/AT Enhanced PS/2 Keyboard (101/102-Key)	
ISA 3	Communications Port (COM2)	
ISA 4	Communications Port (COM1)	
ISA 6	Standard floppy disk controller	
PCI 8	Intel(R) 82845G Graphics Controller	
IRQ 8	System CMOS/real time clock	
ISA 10	MPU-401 Compatible MIDI Device	
ISA 12	Microsoft PS/2 Mouse	
ISA 13	Numeric data processor	
ISA 14	Primary IDE Channel	
ISA 15	Secondary IDE Channel	
PCI 16	Realtek RTL8139 Family PCI Fast Ethernet NIC #2	
PCI 20	Realtek RTL8139 Family PCI Fast Ethernet NIC	
PCI 116	Intel ® 82801DB/DBM USB Universal Host Controller – 24C2	
PCI 117	Intel ® 82801DB/DBM USB Universal Host Controller – 24C4	
PCI 118	Intel ® 82801DB/DBM USB Universal Host Controller – 24C7	
PCI 119	Intel PCI to USB Enhanced Host Controller	
PCI 125	Intel ® 82801DB/DBM USB Universal Host Controller – 24C3	
PCI 125	Realtek AC’97 Audio	

DMA-channel Usage

DMA-channel	Description	Note
DMA2	Standard Floppy Disk Controller	
DMA4	Direct memory access controller	

Appendix C: AWARD BIOS POST Messages

During the Power On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

POST Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and the EISA BIOS.

CMOS Battery Has Failed

CMOS battery is no longer functional. It should be replaced.

CMOS Checksum Error

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

Disk Boot Failure, Insert System Disk And Press Enter

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Diskette Drives Or Types Mismatch Error – Run Setup

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

Display Switch Is Set Incorrectly

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

Display Type Has Changed Since Last Boot

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

EISA Configuration Checksum Error
Please Run EISA Configuration Utility

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the card is installed firmly in the slot.

EISA Configuration Is Not Complete
Please Run EISA Configuration Utility

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note: When either of these errors appear, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Error Encountered initializing Hard Drive

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

Error Initializing Hard Disk Controller

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

Floppy Disk Cntrlr Error Or No Cntrlr Present

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

Invalid EISA Configuration
Please Run EISA Configuration Utility

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Keyboard Error Or No Keyboard Present

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

Memory Address Error At...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Parity Error At...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Size Has Changed Since Last Boot

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

Memory Verify Error At...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

Offending Address Not Found

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

Offending Segment

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

Press A Key To Reboot

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

Press F1 To Disable NMI, F2 To Reboot

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM Parity Error – Checking For Segment...

Indicates a parity error in Random Access Memory.

Should Be Empty But EISA Board Found
Please Run EISA Configuration Utility

A valid board ID was found in a slot that was configured as having no board ID.

NOTE; When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Should Have EISA Board But Not Found
Please Run EISA Configuration Utility

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Slot Not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

System Halted, (CTRL-ALT-DEL) To Reboot...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Wrong Board In Slot
Please Run EISA Configuration Utility

The board ID does not match the ID stored in the EISA non-volatile memory.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Floppy Disk(s) Fail (80) ® Unable To Reset Floppy Subsystem.

Floppy Disk(s) Fail (40) ® Floppy Type Dismatch.

Hard Disk(s) Fail (80) ® HDD Reset Failed

Hard Disk(s) Fail (40) ® HDD Controller Diagnostics Failed.

Hard Disk(s) Fail (20) ® HDD Initialization Error.

Hard Disk(s) Fail (10) ® Unable To Recalibrate Fixed Disk.

Hard Disk(s) Fail (08) ® Sector Verify Failed.

Keyboard Is Locked Out - Unlock The Key.

BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

Keyboard Error Or No Keyboard Present.

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

Manufacturing POST Loop.

System will repeat POST procedure infinitely while the P15 of keyboard controller is pulled low. This is also used for M/B burn in test.

BIOS ROM Checksum Error - System Halted.

The checksum of ROM address F0000H-FFFFFH is bad.

Memory Test Fail.

BIOS reports the memory test fails if the onboard memory is tested error.

Appendix D: AWARD BIOS POST Codes

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.

POST (hex)	Description
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
15h	Reserved
16h	Initial Early_Init_Onboard_Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0.
24h	Reserved
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed. 5. Invoke video BIOS.
2Ah	Reserved

POST (hex)	Description
2Bh	Reserved
2Ch	Reserved
2Dh	1. Initialize multi-language 2. Put information on screen display, including Award title, CPU type, CPU speed ….
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	Reserved
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program writes allocation for AMD K5 CPU.
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved
4Eh	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
4Fh	Reserved

POST (hex)	Description
50h	Initialize USB
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to “AUTO”.
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved

POST (hex)	Description
72h	Reserved
73h	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive. -ALT+F2 is pressed
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..
76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported. -If errors occur, report errors & wait for keys -If no errors occur or F1 key is pressed to continue: ◆Clear EPA or customization logo.
80h	Reserved
81h	Reserved
82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code

POST (hex)	Description
94h	1. Enable L2 cache 2. Program boot up speed 3. Chipset final initialization. 4. Power management final initialization 5. Clear screen & display summary table 6. Program K6 write allocation 7. Program P6 class write combining
95h	1. Program daylight saving 2. Update keyboard LED & typematic rate
96h	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)