# EBM-CN896 Series

**5.25” VIA Eden 1 GHz Mini Module with LVDS, Dual LAN, 2 IEEE1394, CF, 6 USB, 2 SATA, 4 COM & GPIO**

# User’s Manual

**1st Ed – 4 March 2008**

Part No. E2047561700R

## FCC Statement

THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

THESE LIMITS ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST HARMFUL INTERFERENCE WHEN THE EQUIPMENT IS OPERATED IN A COMMERCIAL ENVIRONMENT. THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE HARMFUL INTERFERENCE TO RADIO COMMUNICATIONS.

OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE HARMFUL INTERFERENCE IN WHICH CASE THE USER WILL BE REQUIRED TO CORRECT THE INTERFERENCE AT HIS OWN EXPENSE.

## Notice

This guide is designed for experienced users to setup the system within the shortest time. For detailed information, please always refer to the electronic user's manual.

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**Headquarters**
**Avalue Technology Inc.**
7F, 228, Lian-cheng Road,
Chung Ho City, Taipei,
Taiwan
Tel : +886-2-8226-2345
Fax : +886-2-8226-2777
http://www.avalue.com.tw
E-mail: service@avalue.com.tw

**Europe Branch Office**
**Avalue Europe A/S**
Moelledalen 22C, 3140 Aalsgaarde,,
Denmark
Tel : +45-7025-0310
Fax : +45-4975-5026
http://www.avalue.com.tw
E-mail: service.europe@avalue.com.tw

**China Branch Office**
**Avalue Technology Shanghai Inc.**
Suite A, South 5F, No. 829,
Yisan Road, Caohejing Hi-tech Park,
Shanghai 200233, China
Tel : +86-21-5426-3399
Fax : +86-21-6495-0370
http://www.avalue.com.tw
E-mail: service.china@avalue.com.tw

**US Branch Office**
**Avalue Technology Inc**.
200 Tornillo Way, Suite 210,
Tinton Falls, NJ 07712, USA
Tel: +1-732-578-0200
Fax: +1-732-578-0250
http://www.avalue-usa.com
E-mail: service@avalue-usa.com

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2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information available.
3. If your product is diagnosed as defective, obtain an RMA (return material authorization) number from your dealer. This allows us to process your good return more quickly.
4. Carefully pack the defective product, a complete Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

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# 1. Getting Started

## 1.1 Safety Precautions

**Warning!**

Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

**Always note** that improper disassembling action could cause damage to the motherboard. We suggest not removing the heatsink without correct instructions in any circumstance. If you really have to do this, please contact us for further support.

**Caution!**

Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

## 1.2 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 x EBM-CN896 Eden 1GHz mini module
- 1 x Quick Installation Guide for EBM-CN896
- 1 x DVD-ROM or CD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Audio drivers and utilities

If any of the above items is damaged or missing, contact your retailer.

## 1.3 Document Amendment History

| Revision | Date | By | Comment |
|---|---|---|---|
| 1st | Mar. 2008 | Lingo Tsai | Initial Release |

## 1.4 Manual Objectives

This manual describes in detail the Avalue Technology EBM-CN896 Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with EBM-CN896 series or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

## 1.5 System Specifications

| | |
|---|---|
| **System** | |
| **CPU** | OnBoard VIA V4 Eden 1.0GHz CPU |
| **BIOS** | Award 512 KB Flash BIOS |
| **System Chipset** | VIA CN896 + VT8251 |
| **I/O Chip** | VIA VT1211 |
| **System Memory** | One 240-pin DDR2 SODIMM socket, supports up to 2GB DDR2 400/533/667 SDRAM |
| **SSD** | One CompactFlash Type I/II socket |
| **Watchdog Timer** | Reset: 1~255 min. and 1 sec./step |
| **Expansion** | 1 PC104, 1 PCI Slot |
| **I / O** | |
| **MIO** | 1 x EIDE, 2 x SATA, 4 x RS-232 (4 COM with 40pin Box header. One COM can be set as RS-232/422/485 ), 1 x K/B & Mouse |
| **IrDA** | 115k bps, IrDA 1.0 compliant |
| **USB** | 8 x USB 2.0 ports |
| **Display** | |
| **Chipset** | VIA CN896 with integrated VIA Chrome9 HC DX9 GFX |
| **Resolution** | CRT mode: 1920 x 1440 @ 32 bpp (85 Hz)<br>LCD/Simultaneous mode: 1600 x 1200 @ 16 bpp (60 Hz) |
| **VGA/LCD Interface** | AGP 8X VGA/LCD interface |
| **LVDS** | Dual-channel 18/24-bit LVDS |
| **Audio** | |
| **Chipset** | VIA VT8251 |
| **AC97 Codec** | VIA VT1616 supports 5.1 CH Audio |
| **Audio Interface** | CD Audio in, Mic in, Line in, Line out |
| **Ethernet** | |
| **Chipset** | Dual Realtek RTL8101E |
| **Ethernet Interface** | 10/100/1000Base-T Fast Ethernet compatible |
| **Mechanical & Environmental** | |
| **Power Requirement** | +5V@3.23A, +12V@0.08A, 5VSB@0.08A (with VIA Eden 1GHz & 1GB DDR2 667 SDRAM) |
| **Power Type** | AT/ATX |
| **Operation Temperature** | 0~60® C (32~140® F) |
| **Operating Humidity** | 0%~90% relative humidity, non-condensing |
| **Size ( L x W )** | 8" x 5.75" (203 mm x 146 mm) |
| **Weight** | 0.51 lbs (0.23 kg) |

## 1.6 Architecture Overview

### 1.6.1 Block Diagram

The following block diagram shows the architecture and main components of EBM-CN896 Series.

The following sections provide detail information about the functions provided onboard.

### 1.6.2 VIA CN896 & VT8251

The VIA CN896 chipset supports the VIA V4 Bus to 800MHz, for VIA C7® and VIA Eden™(V4) embedded processors and VIA C7®-D desktop processors, which have been recognized by Microsoft as designed for Windows Vista. It also supports the VIA PowerSaver™ feature, which acts as an automatic transmission to lower or raise the processor's frequency and voltage depending on the workload, reducing overall CPU power consumption by as much as 40 percent.

The VIA CN896 features a high bandwidth VIA Ultra V-Link communication between the chipset's North and South bridges at 533MB/sec. When combined with solutions such as the market-leading VIA VT8237S or VT8251 South Bridges and a broad array of VIA companion chips, the CN896 provides a comprehensive range of storage, multimedia and connectivity features, including native Serial ATA II, support for 6-channel or 8-channel VIA Vinyl Audio, VIA Velocity™ Gigabit Ethernet controllers, wireless LAN connectivity, USB2.0 and IEEE 1394.

Further flexibility can be realized with the availability of one 16-Lane PCI Express port for high end graphics cards and a further 1-Lane PCI Express port for peripheral cards.

The VIA CN896 features a dedicated CRT interface as well as outstanding flexibility for additional video ports such as DVI transmitter, LVDS transmitter, SDTV TV encoder and HDTV TV encoder. This provides customers with the ability to tailor the CN896 to be suitable for use with flat panel displays, a wide variety of LCD panels, TFT color panels, DVI monitors and TV displays. Separate display engines enable two outputs to display at the same time, with different information at different resolutions, pixel depths and refresh rates. The CN896 therefore provides many options for customers designing thin client, industrial PCs, point of sale machines and other embedded product. The inclusion of a 16 lane PCI Express port provides additional upgrade options for desktops, whilst keeping the base configuration at a low cost.

The VIA CN896 chipset features the VIA Chrome9™ HC integrated graphics processor (IGP) featuring a DirectX® 9.0 3D accelerator for high performance and a 2D accelerator for productivity applications.

The 3D graphics engine of the CN896 chipset offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering. This provides stunning image quality without performance loss. The integrated video accelerator also offloads the CPU during MPEG playback.

The Chromotion CE Video Display Engine employs a multi-faceted approach to displaying multimedia content, implementing a number of advanced tools at every stage of video processing. These include integrated MPEG-2 decoding, for flawless digital video playback with ultra-low CPU-utilization, and advanced rendering tools such as Adaptive De-Interlacing and Video Deblocking, which ensure clearer playback of digital content on all

display devices such as CRT, LCD, standard definition TV and HDTV up to 1080p resolution*.

**Key Features**

» Full support for VIA C7, VIA C7-D and VIA Eden (V4) processors
» Supports 667/533/400MHz Front Side Bus Settings
» Supports x16 PCI Express and x1 PCI Express ports
» Supports up to 4GB DDR2 533/400MHz or DDR400/333/266MHz SDRAM
» VIA Ultra V-Link 1 GB/sec 16-bit interconnect supporting V-Map Modular Architecture
» Integrated VIA Chrome9 Graphics core supporting DirectX 9.0 3D graphics
» 250MHz Graphics Engine Clock with separated 128-bit data paths
» 128-bit 2D and 3D Graphics Engine
» Chromotion 3.0 CE Video Display engine
  » MPEG-2 Decoder
  » Video De-blocking
  » Adaptive De-Interlace
  » DuoView+™
  » Full HDTV support up to 1080i / 720p
» Optimized Unified memory Architecture (UMA)
» 12-bit DVI transmitter
» 24-bit Flat Panel Display Interface and Dual 12-bit Flat Panel Display Interface
» 12-bit interface to external TV encoder for SDTV and HDTV display
» Support for VIA Vinyl Gold 8-channel HD Audio Controller & integrated VIA Vinyl 6-channel HD Audio
» Serial ATA support for up to 2 devices
» Integrated V-RAID 0, RAID 1, and RAID 0+1#, and JBOD (SATA) support
» Parallel ATA133/100/66 support for up to 4 devices
» Support for up to 8 USB 2.0/USB 1.1 ports
» Support for VIA Velocity Gigabit Ethernet companion controller & integrated 10/100 Mbps Fast Ethernet
» Advanced System Power Management Support

### 1.6.3 VIA VT1616 AC'97 Codec

VIA Technologies' VT1616TM 18-bit audio codec conforms to the AC'97 2.2 and S/PDIF output specifications. The VT1616 integrates Sample Rate Converters on all channels and can be adjusted in 1Hz increments. There is a provision in hardware for down-mixing the 6 channels into stereo when only two end points are available. The analog mixer circuitry integrates a stereo enhancement to provide a pleasing 3D surround
sound effect for stereo media. This codec is designed with aggressive power management to achieve low power consumption. When used with a 3.3V analog supply, power consumption is further reduced. The primary applications for this part are desktop and portable personal computers multimedia subsystems. However, it is suitable for any

system requiring 6-channel audio output for home theater systems at competitive prices.

- AC'97 2.2 S/PDIF extension compliant codec
- 18-bit, 6 channel DAC outputs
- 1Hz resolution VSR on all channels
- Integrated IEC958 line driver for S/PDIF
- S/PDIF compressed digital or LPCM audio out
- Hardware downmixoption to 2 channels
- 3D stereo expansion for simulated surround
- 18-bit independent rate stereo ADC
- 4 stereo, 2 mono analog line-level inputs
- Second line-level output with volume control
- External Audio Amplifier Control
- Low Power consumption mode
- Exceeds MicrosoftR WHQL logo requirements
- 3.3V digital, 3.3 or 5V analog power supply
- 48-pin LQFP small footprint package

### 1.6.4 VIA VT1636 LVDS Transmitter

- Support Single / Dual LVDS Transmitter Function
- Compatible with TIA/EIA-644 LVDS Standard
- Supports LVDS 18-bit and 24-bit Output
- Supports Dual Channel UXGA Panel Display
- Supports 2D Dither for 18-bit Panel
- Supports Option for 24-bit Color Mapping with Converntional (LSB) or

Non-Conventional (MSB) Format Output

- Supports DVO Input Mode with 25 to 165 MHz Input Clock
- Programmable Input Clock and Strobe Select
- Narrow bus Reduces Cable Size and Cost
- PLL equires No External Components
- Two-Wire Serial Communication
- Panel Protection and Power Down Sequencing
- Panel power Sequencing Control
- Supply Voltage 2.25-2.75V
- 64-pin LQFP Package (10 x 10 x 1.4mm)

### 1.6.5 VIA VT1211 Super I/O

The VT1211 is a full function Super I/O chip with a Floppy Disk Controller, an IEEE-1284 Parallel Port interface, two 16C550-UART-based serial port interfaces, a VFIR (Very Fast IR) Controller, a game port which supports 2 joysticks, a MIDI interface, and a 4M Flash-ROM interface.

The integrated Hardware Monitor Controller controls the speed of 2 fans, monitors 2 fan tachometers, and has a Pentium II thermal diode and 5 universal analog inputs for

measuring voltage or temperature (by connecting external thermistors).

The VT1211 meets the "Microsoft PC98 and PC99 system design guide" requirements and is ACPI ready, and a hardware monitor engine is built in to monitor system health.

**Key Features**

LPC (Low Pin Count) Interface

» Complies with Intel Low Pin Count Interface Specification Revision 1.0

» Supports LDRQ#, SERIRQ protocols

Hardware Monitor Controller

» Built-in 8-bit Analog to Digital Converter

» One thermal input for Pentium II type thermal diode

» 1 intrinsic Vcc voltage monitor input

» 5 external Universal Channels for monitor inputs

» Monitors 2 fan tachometer inputs

» 1 chassis open detection input

» WatchDog comparison of all monitored values

» Provides VID0 - VID4 support for P6 class CPU

» Over temperature indicator output

» Over limit of fan and voltage indicator output

» Provides beep tone warning

» Serial Bus slave mode supported

Fan Speed Controller

» Provides fan on-off and speed control

» Supports 2 programmable Pulse Width Modulation (PWM) outputs

» Duty cycle resolution of 1/256

Flash-ROM Interface

» Supports up to 4MB flash ROM

SmartGuardian Controller

» Provides automatic temperature to fan speed control

» Supports mix-and-match for temperature inputs and fan speed control outputs

» Overrides fan speed controller during catastrophic situations

» Provides over-temperature beep tone warning

Two 16C550 UARTs

» Supports two standard Serial Ports

» Each port supports Serial Port

IEEE1284 Parallel Port

» Standard mode -- Bi-directional SPP

» Enhanced mode -- EPP V1.7 and 1.9 compliant

» High speed mode -- ECP, IEEE1284 compliant

» Backdrive current reduction

» Printer power-on damage reduction

Floppy Disk Controller

» Supports two 360K / 720K / 1.2M / 1.44M / 2.88M floppy disk drives

» Enhanced digital data separator

» 3-Mode drives supported

Game Port

» Built-in 558 quad timers and buffer chips

» Supports direct connection to two joysticks

Dedicated MIDI Interface

» UART implementation

» Supports direct connect to MPU-401 MIDI

56 General Purpose I/O Pins

» Input mode supports switch de-bounce

» Output mode supports one set of programmable LED blinking periods

### 1.6.6 Ethernet

#### 1.6.6.1 Realtek RTL8101E Ethernet Controller

TThe Realtek RTL8101E Fast Ethernet controllers combine an IEEE 802.3 10/100Base-T compliant Media Access Controller (MAC), a PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8100E/RTL8101E offer high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The devices support the PCI Express 1.0a bus interface for host communications with power management and are compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet. They also support an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

The RTL8101E are fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and support IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

**Features**

Integrated 10/100 transceiver

Supports PCI Express™ 1.0

Wake-on-LAN and remote wake-up support

Supports Full Duplex flow control (IEEE 802.3x)

Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab

Supports IEEE 802.1P Layer 2 Priority Encoding

Supports IEEE 802.1Q VLAN tagging

Transmit/Receive on-chip buffer support

Supports power down/link down power saving

Supports PCI Message Signaled Interrupt (MSI)

### 1.6.7 Compact Flash Interface

A Compact Flash type II connector is connected to the secondary IDE controller. The Compact Flash storage card is IDE compatible. It is an ideal replacement for standard IDE hard drives. The solid-state design offers no seek errors even under extreme shock and vibration conditions. The Compact Flash storage card is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage PC card, PDA, and Smart Cellular Phones, allowing simple use for the end user. The Compact Flash storage card is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. The Compact Flash storage card is IDE compatible and offers various capacities.

# 2. Hardware Configuration

## 2.1 Product Overview

## 2.2 Installation Procedure

This chapter explains you the instructions of how to setup your system.

1. Turn off the power supply.
2. Insert the DIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the JFP1.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the "LOAD BIOS DEFAULTS" feature. The ***Integrated Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilized, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

### 2.2.1 Main Memory

EBM-CN896 series provides one 240-pin DIMM socket to support DDR2 SDRAM. The maximum memory size is 2GB.

Make sure to unplug the power supply before adding or removing DIMMs or other system components. Failure to do so may cause severe damage to both the board and the components.

- Locate the DIMM socket on the board.
- Hold two edges of the DIMM module carefully. Keep away of touching its connectors.
- Align the notch key on the module with the rib on the slot.
- Firmly press the modules into the socket automatically snaps into the mounting notch.

Do not force the DIMM module in with extra force as the DIMM module only fit in one direction.

- To remove the DIMM modules, push the two ejector tabs on the slot outward simultaneously, and then pull out the DIMM module.

**Note:** (1) Please do not change any DDR2 SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.

(2) Static electricity can damage the electronic components of the computer or optional boards. Before starting these procedures, ensure that you are discharged of static electricity by touching a grounded metal object briefly.

## 2.3 Jumper and Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.

The jumper settings are schematically depicted in this manual as follows:

A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

The following tables list the function of each of the board's jumpers and connectors.

### Jumpers

| Label | Function | Note |
|---|---|---|
| **JBAT1** | Clear CMOS | 3 x 1 header, pitch 2.54mm |
| **JFP1** | AT/ATX power select & LED indicator Select | 6 x 2 header, pitch 2.54mm |
| **JP1, JP4** | COM2 RS-232/422/485 select | 3x 2 header, pitch 2.0mm |
| **JP2, JP3** | COM2/COM1 pin 9 signal select | 3x 2 header, pitch 2.0mm |

## Connectors

| Label | Function | Note |
|---|---|---|
| **CN1** | System fan connector | 3 x1 wafer, pitch 2.54mm |
| **CN2, 3** | LCD inverter connector for LVDS1 & 2 | 5 x1 wafer, pitch 2.0mm |
| **CN4** | VGA connector | 8 x2 box header, pitch 2.54mm |
| **CN5** | Serial ATA connector 1 | Wafer 7P, pitch 1.27mm |
| **CN6** | Serial ATA connector 2 | Wafer 7P, pitch 1.27mm |
| **CN7, 8** | IEEE 1394 port1 & 2 connector | |
| **CN9** | USB connector 4&5 | 5 x2 header, pitch 2.54mm |
| **CN10** | Audio connector | 8 x2 box header, pitch 2.54mm |
| **CN11** | USB connector 6&7 | 5 x2 header, pitch 2.54mm |
| **CN13** | USB connector 2&3 | 5 x2 header, pitch 2.54mm |
| **CN14** | USB connector 0&1 | 5 x2 header, pitch 2.54mm |
| **CN15, 17** | PC/104 connector | |
| **CN16** | Serial Port 1/2/3/4 connector | 20 x2 box header, pitch2.54mm |
| **CN18** | Keyboard & mouse connector | 4 x2 header, pitch 2.54mm |
| **CN19** | Primary IDE connector | 20x2 box header, pitch 2.54mm |
| **CN20** | CPU fan connector | 3 x1 wafer, pitch 2.54mm |
| **CF1** | Compact Flash connector | |
| **DIMM1** | DDR2 SODIMM 1.8V | 240-pin DDR2 SODIMM socket |
| **DIO1** | General purpose I/O connector | 10 x 2 header, pitch 2.54mm |
| **IR1** | IrDA connector | 5 x 1 header, pitch 2.54mm |
| **JLED1** | LED indicator connector | 4x 2 header, pitch 2.54mm |
| **JLVDS1** | LVDS connector 1 | |
| **JLVDS2** | LVDS connector 2 | |
| **LAN1, 2** | RJ45 Ethernet 1 & 2 | |
| **PCI1** | PCI connector | 60 x 2 header |
| **PLT1** | Parallel port connector | 13 x 2 box header, pitch 2.54mm |
| **PWR1** | ATX power connector | 10 x 2 header, pitch 4.2mm |
| **VR1** | LCD backlight brightness adjustment connector for CN2 | 3 x 1 header, pitch 2.54mm |
| **VR2** | LCD backlight brightness adjustment connector for CN3 | 3 x 1 header, pitch 2.54mm |

## 2.4 Setting Jumpers & Connectors

### 2.4.1 Clear CMOS (JBAT1)

**Protect ***

**Clear CMOS**

*** Default**

### 2.4.2 AT/ATX Power Select & LED Indicator Select (JFP1)

*** Default**

**ATX***

**JFP1 Jumper Settings**

| Signal | PIN |
|---|---|
| HDD LED | 1-3 |
| BUZZER | 2-4 |
| RESET | 5-7 |
| PWR LED | 6-8 |
| PWRBTN | 9-11 |

**Note:** For AT power type, please remove the jumper of Pin 10-12.

### 2.4.3 COM2 RS-232/422/485 Select (JP1, JP4)

(JP1)

RS-232*

RS-422

RS-485

(JP4)

RS-232*

RS-422/485

### 2.4.4 COM1 Pin 9 Signal Select for COM2 (JP2)

Ring*

+5V

+12V

*** Default**

### 2.4.5 COM1 Pin 9 Signal Select for COM1 (JP3)

*** Default**

### 2.4.6 System Fan Connector (CN1)

| Signal | PIN |
|---|---|
| +5V | 3 |
| +12V | 2 |
| GND | 1 |

### 2.4.7 LCD Inverter Connector for LVDS1 & 2 (CN2, CN3)

| Signal | PIN |
|---|---|
| +12V | 1 |
| GND | 2 |
| ENBKL | 3 |
| VR | 4 |
| +5V | 5 |

**Note:**

For inverters with adjustable Backlight function, it is possible to control the LCD brightness through the VR signal controlled by **VR1 & VR2**. Please see the VR1 for CN2 or VR2 for CN3 section for detailed circuitry information.

#### 2.4.7.1 Signal Description – LCD Inverter Connector (JBKL1)

| Signal | Signal Description |
|---|---|
| VR | Vadj = 0.75V ~ 4.25V (Recommended: 4.7KΩ, >1/16W) |
| ENBKL | LCD backlight ON/OFF control signal |

## 2.4.8 VGA Connector (CN4)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| R | 1 | 2 | +5V |
| G | 3 | 4 | GND |
| B | 5 | 6 | NC |
| NC | 7 | 8 | DAT |
| GND | 9 | 10 | HS |
| GND | 11 | 12 | VS |
| GND | 13 | 14 | DCK |
| GND | 15 | 16 | NC |

### 2.4.8.1 Signal Description – VGA Connector (CN4)

| Signal | Signal Description |
|---|---|
| HS, VS | CRT horizontal / vertical synchronisation output |
| DCK | Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface. |
| DAT | Display Data Channel Data. Used as data signal to/from monitors with DDC interface. |
| R, G, B | Analog output carrying the red / green / blue colour signal to the CRT. For 75 Ω cable impedance. |

### 2.4.9 USB Connector 4 & 5 (CN9)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| +5V | 1 | 2 | GND |
| D4- | 3 | 4 | GND |
| D4+ | 5 | 6 | D5+ |
| GND | 7 | 8 | D5- |
| GND | 9 | 10 | +5V |

#### 2.4.9.1 Signal Description – USB Connecter 4 & 5 (CN9)

| Signal | Signal Description |
|---|---|
| D4+ / D4- | Differential bi-directional data signal for USB channel 4. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs. |
| D5+ / D5- | Differential bi-directional data signal for USB channel 5. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs. |

## 2.4.10 Audio Connector (CN10)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| MIC IN | 1 | 2 | MIC VREF |
| AUDGND | 3 | 4 | AUDGND |
| LINEOUT L | 5 | 6 | LINEOUT R |
| NC | 7 | 8 | NC |
| LINEIN L | 9 | 10 | LINEIN R |
| AUDGND | 11 | 12 | NC |
| GND | 13 | 14 | NC |
| GND | 15 | 16 | NC |

### 2.4.10.1 Signal Description – Audio Connector (CN10)

| Signal | Signal Description |
|---|---|
| MIC IN | The MIC signal is used for microphone input. This input is fed to the left microphone channel. |
| MIC VREF | VREF is a voltage out reference for Mic |
| LINEOUT L/R | Left and right speaker output. These are the speaker outputs directly from the speaker amplifier. |
| LINEIN L/R | Left and right line in signals. |

### 2.4.11 USB Connector 6 & 7 (CN11)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| +5V | 1 | 2 | GND |
| D6- | 3 | 4 | GND |
| D6+ | 5 | 6 | D7+ |
| GND | 7 | 8 | D7- |
| GND | 9 | 10 | +5V |

#### 2.4.11.1 Signal Description – USB Connecter 6 & 7 (CN11)

| Signal | Signal Description |
|---|---|
| D6+ / D6- | Differential bi-directional data signal for USB channel 6. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs. |
| D7+ / D7- | Differential bi-directional data signal for USB channel 7. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs. |

## 2.4.12 USB Connector 2 & 3 (CN13)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| +5V | 1 | 2 | GND |
| D2- | 3 | 4 | GND |
| D2+ | 5 | 6 | D3+ |
| GND | 7 | 8 | D3- |
| GND | 9 | 10 | +5V |

### 2.4.12.1 Signal Description – USB Connecter 2 & 3 (CN9)

| Signal | Signal Description |
|---|---|
| D2+ / D2- | Differential bi-directional data signal for USB channel 2. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs. |
| D3+ / D3- | Differential bi-directional data signal for USB channel 3. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs. |

### 2.4.13 USB Connector 0 & 1 (CN14)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| +5V | 1 | 2 | GND |
| D0- | 3 | 4 | GND |
| D0+ | 5 | 6 | D1+ |
| GND | 7 | 8 | D1- |
| GND | 9 | 10 | +5V |

#### 2.4.13.1 Signal Description – USB Connecter 2 & 3 (CN9)

| Signal | Signal Description |
|---|---|
| D0+ / D0- | Differential bi-directional data signal for USB channel 0. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs. |
| D1+ / D1- | Differential bi-directional data signal for USB channel 1. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs. |

### 2.4.14 PC/104 Connector (CN15 + CN17)

**CN15**

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| GND | B32 | A32 | GND |
| GND | B31 | A31 | SA0 |
| OSC | B30 | A30 | SA1 |
| +5V | B29 | A29 | SA2 |
| BALE | B28 | A28 | SA3 |
| TC | B27 | A27 | SA4 |
| DACK2# | B26 | A26 | SA5 |
| IRQ3 | B25 | A25 | SA6 |
| IRQ4 | B24 | A24 | SA7 |
| IRQ5 | B23 | A23 | SA8 |
| IRQ6 | B22 | A22 | SA9 |
| IRQ7 | B21 | A21 | SA10 |
| SYS_CLK | B20 | A20 | SA11 |
| REFRESH# | B19 | A19 | SA12 |
| DRQ1 | B18 | A18 | SA13 |
| DACK1# | B17 | A17 | SA14 |
| DRQ3 | B16 | A16 | SA15 |
| DACK3# | B15 | A15 | SA16 |
| IOR# | B14 | A14 | SA17 |
| IOW# | B13 | A13 | SA18 |
| SMEMR# | B12 | A12 | SA19 |
| SMEMW# | B11 | A11 | AEN |
| GND | B10 | A10 | IOCHRDY |
| +12V | B9 | A9 | SD0 |
| OWS# | B8 | A8 | SD1 |
| -12V | B7 | A7 | SD2 |
| DRQ2 | B6 | A6 | SD3 |
| -5V | B5 | A5 | SD4 |
| IRQ9 | B4 | A4 | SD5 |
| +5V | B3 | A3 | SD6 |
| RESETDRV | B2 | A2 | SD7 |
| GND | B1 | A1 | IOCHK# |

**CN17**

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| NC | C20 | D20 | GND |
| SD15 | C19 | D19 | GND |
| SD14 | C18 | D18 | MASTER# |
| SD13 | C17 | D17 | +5V |
| SD12 | C16 | D16 | DRQ7 |
| SD11 | C15 | D15 | DACK7# |
| SD10 | C14 | D14 | DRQ6 |
| SD9 | C13 | D13 | DACK6# |
| SD8 | C12 | D12 | DRQ5 |
| MEMW# | C11 | D11 | DACK5# |
| MEMR# | C10 | D10 | DRQ0 |
| SA17 | C9 | D9 | DACK0# |
| SA18 | C8 | D8 | IRQ14 |
| SA19 | C7 | D7 | IRQ15 |
| LA20 | C6 | D6 | IRQ12 |
| LA21 | C5 | D5 | IRQ11 |
| LA22 | C4 | D4 | IRQ10 |
| LA23 | C3 | D3 | IOCS16# |
| SBHE# | C2 | D2 | MEMCS16# |
| GND | C1 | D1 | GND |

### 2.4.14.1 Signal Description –PC/104 Connector (CN15 + CN17)

#### 2.4.14.1.1 ddress

| Signal | Signal Description |
|---|---|
| LA [17:23] | The address signals LA [23:17] define the selection of a 128KB section of memory space within the 16MB address range of the 16-bit data bus. These signals are active high. The validity of the MEMCS16# depends on these signals only. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case, the temporary master drives these lines. The LA signals are not defined for I/O accesses. |

| | |
|---|---|
| SA [0:19] | System address. Address lines for the first one Megabyte of memory. SA [9:0] used for I/O addresses. SA0 is the least significant bit |
| SBHE# | This signal is an active low signal, that indicates that a byte is being transferred on the upper byte (SD [15:8]) of the 16 bit bus. All bus masters will drive this line with a tri-state driver. |

### 2.4.14.1.2 Data

<table>
<tr><th>Signal</th><th>Signal Description</th></tr>
<tr><td>SD [0:7]</td><td>These signals are defined for the low order byte of the 16-bit data bus being the only bus for 8 bit PC-AT/PC104 adapter boards. Memory or I/O transfers on this part of the data bus are defined for 8-bit operations with even or odd addresses and for 16-bit operations for odd addresses only. The signals SA0 and SBHE# are used to define the data present on this bus:
<table>
<tr><th>SBHE#</th><th>SA0</th><th>SD8-SD15</th><th>SD0-SD7</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>ODD</td><td>EVEN</td><td>Word transfer</td></tr>
<tr><td>0</td><td>1</td><td>ODD</td><td>ODD</td><td>Byte transfer on SD8-SD15</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>EVEN</td><td>Byte transfer on SD0-SD7</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>ODD</td><td>Byte transfer on SD7-</td></tr>
</table></td></tr>
<tr><td>SD [8:15]</td><td>These signals are defined for the high order byte of the 16-bit data bus. Memory or I/O transfers on this part of the bus are defined when SBHE# is active.</td></tr>
</table>

### 2.4.14.1.3 Commands

| Signal | Signal Description |
|---|---|
| BALE | This is an active high signal used to latch valid addresses from the current bus master on the falling edge of BALE. During DMA, refresh and alternate master cycles, BALE is forced high for the duration of the transfer. BALE is driven by the permanent master with a totem-pole driver. |
| IOR# | This is an active low signal driven by the current master to indicate an I/O read operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with DACKn# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver. |
| IOW# | This is an active low signal driven by the current master to indicate an I/O write operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with DACKn# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver. |
| SMEMR# | This is an active low signal driven by the permanent master to indicate a memory read operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters. |
| SMEMW# | This is an active low signal driven by the permanent master to indicate a memory write operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters. |
| MEMR# | This is an active low signal driven by the current master to indicate a memory read operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters. |
| MEMW# | This is an active low signal driven by the current master to indicate a memory write operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters. |

### 2.4.14.1.4 Transfer Response

| Signal | Signal Description |
|---|---|
| IOCS16# | This is an active low signal driven by an I/O-mapped PC-AT/PC104 adapter indicating that the I/O device located at the address is a 16-bit device. This open collector signal is driven, based on SA [15:0] only (not IOR# and IOW#) when AEN is not asserted. |
| MEMCS16# | This is an active low signal driven by a memory mapped PC-AT/PC104 adapter indicating that the memory device located at the address is a 16-bit device. This open collector signal is driven, based on LA [23:17] only. |
| OWS# | This signal is an active low open-collector signal asserted by a 16-bit memory mapped device that may cause an early termination of the current transfer. It should be gated with MEMR# or MEMW# and is not valid during DMA transfers. IOCHRDY precedes 0WS#. |
| IOCHRDY | This is an active high signal driven inactive by the target of either a memory or an I/O operation to extend the current cycle. This open collector signal is driven based on the system address and the appropriate control strobe. IOCHRDY precedes 0WS#. |
| IOCHCK# | This is an active low signal driven active by a PC-AT/PC104 adapter detecting a fatal error during bus operation. When this open collector signal is driven low it will typically cause a non-maskable interrupt. |

### 2.4.14.1.5 Control

| Signal | Signal Description |
|---|---|
| SYSCLK | This clock signal may vary in frequency from 2.5 MHz to 25.0 MHz depending on the setup made in the BIOS. Frequencies above 16 MHz are not recommended. The standard states 6 MHz to 8.33 MHz, but most new adapters are able to handle higher frequencies. The PC-AT/PC104 bus timing is based on this clock signal. |
| OSC | This is a clock signal with a 14.31818 MHz ± 50 ppm frequency and a 50 ± 5% duty cycle. The signal is driven by the permanent master. |
| RESETDRV | This active high signal indicates that the adapter should be brought to an initial reset condition. This signal will be asserted by the permanent master on the bus for at least 100 ms at power-up or watchdog time-out to ensure that adapters in the system are properly reset. When active, all adapters should turn off or tri-state all drivers connected to the bus. |

### 2.4.14.1.6 Interrupts

| Signal | Signal Description |
|---|---|
| IRQ[3:7], IRQ[9:12] IRQ[14:15] | These signals are active high signals, which indicate the presence of an interrupting PC-AT/PC104 bus adapter. Due to the use of pull-ups, unused interrupt inputs must be masked. |

### 2.4.14.1.7 Bus Arbitration

| Signal | Signal Description |
|---|---|
| DRQ[0:3], DRQ[5:7] | These signals are active high signals driven by a DMA bus adapter to indicate a request for a DMA bus operation. DRQ [0:3] request 8 bit DMA operations, while DRQ [5:7] request 16 bit operations. All bus DMA adapters will drive these lines with a tri-state driver. The permanent master monitors these signals to determine which of the DMA devices, if any, are requesting the bus. |
| DACK[0:3]#, DACK[5:7]# | These signals are active low signals driven by the permanent master to indicate that a DMA operation can begin. They are continuously driven by a totem pole driver for DMA channels attached. |
| AEN | This signal is an active high totem pole signal driven by the permanent master to indicate that the address lines are driven by the DMA controller. The assertion of AEN disables response to I/O port addresses when I/O command strobes are asserted. AEN being asserted, only the device with active DACKn# should respond. |
| REFRESH# | This is an active low signal driven by the current master to indicate a memory refresh operation. The current master will drive this line with a tri-state driver. |
| TC | This active high signal is asserted during a read or write command indicating that the DMA controller has reached a terminal count for the current transfer. DACKn# must be presented by the bus adapter to validate the TC signal. |
| MASTER# | This signal is not supported by the chipset. |

## 2.4.15 Serial Port 1/2/3/4 Connector (CN16)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| DCDA | 1 | 2 | DSRA |
| RXDDA | 3 | 4 | RTSA |
| TXDDA | 5 | 6 | CTSA |
| DTRA | 7 | 8 | RIA |
| GND | 9 | 10 | NC |
| CM2-1 | 11 | 12 | DSRB |
| CM2-2 | 13 | 14 | RTSB |
| CM2-3 | 15 | 16 | CTSB |
| CM2-4 | 17 | 18 | RIB |
| GND | 19 | 20 | NC |
| DCD3# | 21 | 22 | DSR3# |
| RXDD3 | 23 | 24 | RTS3# |
| TXDD3 | 25 | 26 | CTS3# |
| DTR3# | 27 | 28 | RI3# |
| GND | 29 | 30 | NC |
| DCD4# | 31 | 32 | DSR4# |
| RXDD4 | 33 | 34 | RTS4# |
| TXDD4 | 35 | 36 | CTS4# |
| DTR4# | 37 | 38 | RI4# |
| GND | 39 | 40 | NC |

### 2.4.15.1 Serial Port 1/2/3/4 Connector (CN16)

| Signal | Signal Description |
|---|---|
| TxD | Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated. |
| RxD | Serial input. This signal receives serial data from the communication link. |
| DTR | Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link. |
| DSR | Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link. |
| RTS | Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data. |
| CTS | Clear To Send. This signal indicates that the modem or data set is ready to exchange data. |
| DCD | Data Carrier Detect. This signal indicates that the modem or data set has |

| | |
|---|---|
| | detected the data carrier. |
| RI | Ring Indicator. This signal indicates that the modem has received a telephone ringing signal. |

### 2.4.16 Keyboard & Mouse Connector (CN18)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| KDAT | 1 | 2 | KCLK |
| GND | 3 | 4 | +5V |
| MDAT | 5 | 6 | MCLK |
| NC | 7 | 8 | NC |

#### 2.4.16.1 Signal Description – Keyboard & Mouse Connector (CN18)

| Signal | Signal Description |
|---|---|
| KCLK | Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard. |
| KDAT | Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard. |
| MCLK | Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse. |
| MDAT | Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse. |

### 2.4.17 Primary IDE Connector (CN19)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| RESET# | 1 | 2 | GND |
| PDD7 | 3 | 4 | PDD8 |
| PDD6 | 5 | 6 | PDD9 |
| PDD5 | 7 | 8 | PDD10 |
| PDD4 | 9 | 10 | PDD11 |
| PDD3 | 11 | 12 | PDD12 |
| PDD2 | 13 | 14 | PDD13 |
| PDD1 | 15 | 16 | PDD14 |
| PDD0 | 17 | 18 | PDD15 |
| GND | 19 | 20 | NC |
| PDREQ | 21 | 22 | GND |
| PDIOW# | 23 | 24 | GND |
| PDIOR# | 25 | 26 | GND |
| PIORDY | 27 | 28 | GND |
| PDDACK# | 29 | 30 | GND |
| IRQ14 | 31 | 32 | NC |
| PDA1 | 33 | 34 | NC |
| PDA0 | 35 | 36 | PDA2 |
| PDCS1# | 37 | 38 | PDCS3# |
| IDEACTP# | 39 | 40 | GND |

#### 2.4.17.1 Signal Description – Primary IDE Connector (CN19)

| Signal | Signal Description |
|---|---|
| PDA [2:0] | IDE Address Bits. These address bits are used to access a register or data port in a device on the IDE bus. |
| PDCS1#, PDCS3# | IDE Chip Selects. The chip select signals are used to select the command block registers in an IDE device. DCS1# selects the primary hard disk. |
| PDD [15:0] | IDE Data Lines. D [15:0] transfers data to/from the IDE devices. |
| PDIOR# | IDE I/O Read. Signal is asserted on read accesses to the corresponding IDE port addresses. |

| | |
|---|---|
| PDIOW# | IDE I/O Write. Each signal is asserted on write accesses to corresponding the IDE port addresses. |
| PIORDY | When deasserted, these signals extend the transfer cycle of any host register access when the device is not ready to respond to the data transfer request. |
| RESET# | IDE Reset. This signal resets all the devices that are attached to the IDE interface. |
| IRQ14 | Interrupt line from hard disk. Connected directly to PC-AT bus. |
| PDREQ | The DREQ is used to request a DMA transfer from the South Bridge. The direction of the transfers is determined by the IOR#/IOW# signals. |
| PDDACK# | DMA Acknowledge. The DACK# acknowledges the DREQ request to initiate DMA transfers. |
| IDEACTP# | Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signal is routed directly to the LED. |

### 2.4.18 CPU Fan Connector (CN20)

| Signal | PIN |
|---|---|
| +5V | 3 |
| +12V | 2 |
| GND | 1 |

## 2.4.19 General Purpose I/O Connector (DIO1)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| +5V | 20 | 19 | GND |
| SMB_DATA_S | 18 | 17 | SMB_CLK_S |
| DI_GP17 | 16 | 15 | DO_GP27 |
| DI_GP16 | 14 | 13 | DO_GP26 |
| DI_GP15 | 12 | 11 | DO_GP25 |
| DI_GP14 | 10 | 9 | DO_GP24 |
| DI_GP13 | 8 | 7 | DO_GP23 |
| DI_GP12 | 6 | 5 | DO_GP22 |
| DI_GP11 | 4 | 3 | DO_GP21 |
| DI_GP10 | 2 | 1 | DO_GP20 |

### 2.4.19.1 General Purpose I/O Connector (DIO1)

| Signal | Signal Description |
|---|---|
| DI [7:0] | Digital Input Data Bit 7 to Bit 0 |
| DO [7:0] | Digital Output Data Bit 7 to Bit 0 |
| SM_CLK_S | Data input for $I^2C$ input, 5V tolerant |
| SM_DATA_S | Data input for $I^2C$ serial input, 5V tolerant |

### 2.4.20 IrDA Connector (IR1)

| Signal | PIN |
|---|---|
| +5V | 1 |
| NC | 2 |
| IRRX | 3 |
| GND | 4 |
| IRTX | 5 |

#### 2.4.20.1 Signal Description – IrDA Connecter (IR1)

| Signal. | Signal Description |
|---|---|
| IRRX | Infrared Receiver input |
| IRTX | Infrared Transmitter output |

## 2.4.21 LED Indicator Connector (JLED1)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| PCIE1_S1000 | 1 | 2 | LAN2_S1000 |
| PCIE1_S100 | 3 | 4 | LAN2_S100 |
| PCIE1_ACT | 5 | 6 | LAN2_ACT |
| +3.3V | 7 | 8 | +3.3V |

### 2.4.21.1 Signal Description – LED Indicator Connector (JLED1)

| Signal | Signal Description |
|---|---|
| PCIE_ACT, LAN2_ACT | Activity LED. The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off. |
| PCIE_S1000, LAN2_S1000, | Speed LED. The Speed LED pin indicates the speed. The speed LED will be on at 1000 Mbps |
| PCIE_S100, LAN2_S100 | Speed LED. The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps. |

### 2.4.22 LVDS Connector 1 & 2 (JLVDS1, JLVDS2)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| +5V | 2 | 1 | +3.3V |
| +5V | 4 | 3 | +3.3V |
| $I^2C$_DAT | 6 | 5 | $I^2C$_CLK |
| GND | 8 | 7 | GND |
| Txout0 | 10 | 9 | Txout1 |
| Txout0# | 12 | 11 | Txout1# |
| GND | 14 | 13 | GND |
| Txout2 | 16 | 15 | Txout3 |
| Txout2# | 18 | 17 | Txout3# |
| GND | 20 | 19 | GND |
| E_Txout0 | 22 | 21 | E_Txout1 |
| E_Txout0# | 24 | 23 | E_Txout1# |
| GND | 26 | 25 | GND |
| E_Txout2 | 28 | 27 | E_Txout3 |
| E_Txout2# | 30 | 29 | E_Txout3# |
| GND | 32 | 31 | GND |
| Txclk | 34 | 33 | E_Txclk |
| Txclk# | 36 | 35 | E_Txclk# |
| GND | 38 | 37 | GND |
| NC | 40 | 39 | NC |

#### 2.4.22.1 Signal Description – LVDS Connecter (JLVDS1, JLVDS2)

| Signal | Description |
|---|---|
| $I^2C$_DAT, $I^2C$_CLK | $I^2C$ interface for panel parameter EEPROM. This EERPOM is mounted on the LVDS receiver. The data in the EEPROM allows the EXT module to automatically set the proper timing parameters for a specific LCD panel. |

### 2.4.23 Parallel Port Connector (PLT1)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| STB# | 1 | 2 | AFD# |
| PD0 | 3 | 4 | ERR# |
| PD1 | 5 | 6 | INIT# |
| PD2 | 7 | 8 | SLIN# |
| PD3 | 9 | 10 | GND |
| PD4 | 11 | 12 | GND |
| PD5 | 13 | 14 | GND |
| PD6 | 15 | 16 | GND |
| PD7 | 17 | 18 | GND |
| ACK# | 19 | 20 | GND |
| BUSY | 21 | 22 | GND |
| PE | 23 | 24 | GND |
| SLCT | 25 | 26 | GND |

### 2.4.23.1 Signal Description – Parallel Port Connecter (PLT1)

| Signal | Signal Description |
|---|---|
| PD[7:0] | Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode. |
| SLIN# | Output line for detection of printer selection. This pin is pulled high internally. |
| SLCT | An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. |
| STB# | An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. |
| BUSY | An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. |
| ACK# | An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. |
| INIT# | Output line for the printer initialization. This pin is pulled high internally. |
| AFD# | An active low output from this pin causes the printer to auto feed a line after a line is printed.<br>This pin is pulled high internally. |
| ERR# | An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. |
| PE | An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. |

### 2.4.24 ATX Power Connector (PWR1)

| Signal | PIN | PIN | Signal |
|---|---|---|---|
| +12V | 10 | 20 | +5V |
| +5VSB | 9 | 19 | +5V |
| NC | 8 | 18 | NC |
| GND | 7 | 17 | GND |
| +5V | 6 | 16 | GND |
| GND | 5 | 15 | GND |
| +5V | 4 | 14 | PS_ON |
| GND | 3 | 13 | GND |
| NC | 2 | 12 | NC |
| NC | 1 | 11 | NC |

### 2.4.25 LCD Backlight Brightness Adjustment Connector (VR1)

| Signal | PIN |
|---|---|
| +5V | 1 |
| VR | 2 |
| GND | 3 |

Variation Resistor

(Recommended: 4.7KΩ, >1/16W)

### 2.4.26 LCD Backlight Brightness Adjustment Connector (VR2)

| Signal | PIN |
|---|---|
| +5V | 1 |
| VR | 2 |
| GND | 3 |

Variation Resistor

(Recommended: 4.7KΩ, >1/16W)

# 3 BIOS Setup

## 3.1 Starting Setup

The AwardBIOS™ is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing <Del> immediately after switching the system on, or

By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

**Press DEL to enter SETUP**

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

**Press F1 to Continue, DEL to enter SETUP**

## 3.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

| Button | Description |
|---|---|
| ↑ | Move to previous item |
| ↓ | Move to next item |
| ← | Move to the item in the left hand |
| → | Move to the item in the right hand |
| Esc key | Main Menu -- Quit and not save changes into CMOS<br>Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu |
| PgUp key | Increase the numeric value or make changes |
| PgDn key | Decrease the numeric value or make changes |
| + key | Increase the numeric value or make changes |
| - key | Decrease the numeric value or make changes |
| F1 key | General help, only for Status Page Setup Menu and Option Page Setup Menu |
| (Shift) F2 key | Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward |
| F3 key | Calendar, only for Status Page Setup Menu |
| F4 key | Reserved |
| F5 key | Restore the previous CMOS value from CMOS, only for Option Page Setup Menu |
| F6 key | Load the default CMOS value from BIOS default table, only for Option Page Setup Menu |
| F7 key | Load the default |
| F8 key | Reserved |
| F9 key | Reserved |
| F10 key | Save all the CMOS changes, only for Main Menu |

- **Navigating Through The Menu Bar**

Use the left and right arrow keys to choose the menu you want to be in.

**Note:** Some of the navigation keys differ from one screen to another.

- **To Display a Sub Menu**

Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A "➢" pointer marks all sub menus.

## 3.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

## 3.4 In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

## 3.5 Main Menu

Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

Note that a brief description of each highlighted selection appears at the bottom of the screen.

**Note:** The BIOS setup screens shown in this chapter are for reference purposes only, and may not exactly match what you see on your screen.
Visit the Avalue website (www.avalue.com.tw) to download the latest product and BIOS information.

### 3.5.1 Standard CMOS Features

The items in Standard CMOS Setup Menu are divided into few categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.

#### 3.5.1.1 Main Menu Selection

This reference table shows the selections that you may make on the Main Menu.

| Item | Options | Description |
|---|---|---|
| Date | MM DD YYYY | Set the system date. Note that the 'Day' automatically changes when you set the date |
| Time | HH : MM : SS | Set the system time |
| IDE Channel 0 Master<br>IDE Channel 0 Slave<br>IDE Channel 1 Master | Options are in 3.5.1.2 | Press <Enter> to enter the sub menu of detailed options |
| Video | EGA/VGA<br>CGA 40<br>CGA 80<br>MONO | Select the default video device |
| Halt On | All Errors<br>No Errors<br>All, but Keyboard | Select the situation in which you want the BIOS to stop the POST process and notify you |

### 3.5.1.2 IDE Adapter Setup

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive. The below Figure will shows the IDE primary master sub menu.

| Item | Options | Description |
|---|---|---|
| IDE HDD Auto-detection | Press Enter | Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu. |
| IDE Channel 0 Master<br>IDE Channel 0 Slave<br>IDE Channel 1 Master | None<br>Auto<br>Manual | Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE ! |
| Access Mode | CHS<br>LBA<br>Large<br>Auto | Choose the access mode for this hard disk |
| The following options are selectable only if the 'IDE Channel …' item is set to 'Manual' | | |
| Cylinder | Min = 0<br>Max = 65535 | Set the number of cylinders for this hard disk. |
| Head | Min = 0<br>Max = 255 | Set the number of read/write heads |
| Precomp | Min = 0<br>Max = 65535 | **** **Warning**: Setting a value of 65535 means no hard disk |
| Landing zone | Min = 0<br>Max = 65535 | This setting specifies the cylinder to which the BIOS should send the heads of the hard disk when the machine is to be turned off. IDE autodetection will set this value automatically. |
| Sector | Min = 0<br>Max = 255 | Number of sectors per track |

### 3.5.2 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.

```
Phoenix - AwardBIOS CMOS Setup Utility
Advanced BIOS Features

▶ CPU Feature                  [Press Enter]        Item Help
▶ Hard Disk Boot Priority      [Press Enter]
  Virus Warning                [Disabled]           Menu Level  ▶
  CPU L1 & L2 Cache            [Enabled]
  CPU L3 Cache                 [Enabled]
  CPU L2 Cache ECC Checking    [Enabled]
  Quick Power On Self Test     [Enabled]
  First Boot Device            [Hard Disk]
  Second Boot Device           [CDROM]
  Third Boot Device            [LS120]
  Boot Other Device            [Enabled]
  Boot Up NumLock Status       [On]
  Typematic Rate Setting       [Disabled]
x Typematic Rate (Chars/Sec) 6
x Typematic Delay (Msec)      250
  Security Option              [Setup]
  MPS Version Control For OS[1.4]
  OS Select For DRAM > 64MB [Non-OS2]
  HDD S.M.A.R.T. Capability [Disabled]

↑↓→←:Move  Enter:Select  +/-/PU/PD:Value  F10:Save  ESC:Exit  F1:General Help
  F5: Previous Values    F6: Fail-Safe Defaults    F7: Optimized Defaults
```

#### 3.5.2.1 CPU Features

```
Phoenix - AwardBIOS CMOS Setup Utility
CPU Feature

  Delay Prior to Thermal     [16 Min]             Item Help
  Thermal Management         [Thermal Monitor 1]
  Thermal Monitor Bus Ratio  [ 0 X]               Menu Level  ▶
  Thermal Monitor Bus VID    [0.700V]

↑↓→←:Move  Enter:Select  +/-/PU/PD:Value  F10:Save  ESC:Exit  F1:General Help
  F5: Previous Values    F6: Fail-Safe Defaults    F7: Optimized Defaults
```

| Item | Options | Description |
|---|---|---|
| Delay Prior to Thermal | 4 Min, 8 Min,<br>16 Min, 32 Min | This item is to set whether to run Delay Prior to Thermal. |
| Thermal Management | Thermal Monitor 1<br>Thermal Monitor 2<br>Thermal Monitor 3 | Allow you to choose the thermal management method of your monitor. |
| TM2 Bus Ratio | Min = 0<br>Max = 255 | This item is to set the frequency (bus ratio) of the throttled performance that will be initiated when the on die sensor goes from not hot to hot |
| TM2 Bus VID | 0.700 ~ 1.708 | This item is to set the voltage of the throttled performance that will be initiated when the on die sensor goes from not hot to hot. |

### 3.5.2.2 Hard Disk boot Priority

This item allows you to select the Hard Disk device boot up priority.

| Item | Description |
|---|---|
| Pri.Master | Boot up from IDE Primary Master Hard Disk |
| Pri.Slave | Boot up from IDE Primary Slave Hard Disk |
| Sec.Master | Boot up from IDE Secondary Master Hard Disk |
| Sec.Slave | Boot up from IDE Secondary Slave Hard Disk |
| USBHDD0 | Boot up from First USB Hard Disk |
| USBHDD1 | Boot up from Second USB Hard Disk |
| USBHDD2 | Boot up from Thrid USB Hard Disk |
| Bootable Add-in Cards | Boot up from other Add-In Card Hard Disk Device. |

### 3.5.2.3 Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

| Item | Description |
|---|---|
| Enabled | Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table. |
| Disabled | No warning message will appear when anything attempts to access the boot sector or hard disk partition table. |

### 3.5.2.4 CPU L1 ,L2 & L3 Cache

Depending on the CPU/chipset in use, you may be able to increase memory access time with this option.

| Item | Description |
|---|---|
| Enabled | Enable cache |
| Disabled | Disable cache |

### 3.5.2.5 CPU L2 Cache ECC Checking

This item allows you to enable the CPU external L2 cache use ECC checking method in memory access.

| Item | Description |
|---|---|
| Enabled | Enable ECC checking |
| Disabled | Disable ECC checking |

### 3.5.2.6 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

| Item | Description |
|---|---|

| | |
|---|---|
| Enabled | Enable quick POST |
| Disabled | Normal POST |

#### 3.5.2.7 First / Second / Third / Other Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

| Item | Description |
|---|---|
| LS120 | LS120 Device |
| Hard Disk | Hard Disk Device |
| CDROM | CDROM Device |
| ZIP100 | ZIP-100 Device |
| USB-FDD | USB Floppy Device |
| USB-ZIP | USB ZIP Device |
| USB-CDROM | USB CDROM Device |
| Legacy LAN | Network Device |
| Disabled | Disabled any boot device |

#### 3.5.2.8 Boot Up NumLock Status

Select power on state for NumLock.

| Item | Description |
|---|---|
| On | Enable NumLock |
| Off | Disable NumLock |

#### 3.5.2.9 Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

| Item | Description |
|---|---|
| Enabled | Enable typematic rate/delay setting |
| Disabled | Disable typematic rate/delay setting |

#### 3.5.2.10 Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a key stroke when you hold the key down. The choice: 6, 8, 10, 12, 15, 20, 24, 30.

#### 3.5.2.11 Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke. The choice: 250, 500, 750, 1000.

#### 3.5.2.12 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

| Item | Description |
|---|---|
| System | The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt. |
| Setup | The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt. |

**Note:** To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

#### 3.5.2.13 MPS Version Control For OS

This feature is only applicable to multiprocessor board as it specifies the version of the Multi-Processor Specification (MPS) that the board will use.

The choice: 1.4, 1.1.

#### 3.5.2.14 OS Select for DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.

| Item | Description |
|---|---|
| Non-OS2 | Disable OS for over 64 MB DRAM |
| OS2 | Enable OS for over 64 MB DRAM |

#### 3.5.2.15 HDD S.M.A.R.T. Capability

S.M.A.R.T.(Self Monitoring Analysis and Reporting Technology) is supported by all current hard disks and it allows the early prediction and warning of impending hard disk disasters. You should enable it if you want to use S.M.A.R.T.-aware utilities to monitor the hard disk's condition. Enabling it also allows the monitoring of the hard disk's condition over a network.

| Item | Description |
|---|---|
| Enable | Enable for hard disk’s monitoring condition |
| Disable | Disable for hard disk’s monitoring condition |

#### 3.5.2.16 Video BIOS Shadow

To allow copying Video BIOS into shadow RAM to improve video performance.

| Item | Description |
|---|---|
| Enable | Copy Video BIOS into shadow RAM |
| Disable | Do not copy Video BIOS into shadow RAM |

#### 3.5.2.17 Full Screen LOGO Show

If the BIOS had the full screen logo in it, this item could allow enable/ disable the full screen logo show on display.

| Item | Description |
|---|---|
| Enable | Enable full screen logo show |
| Disable | Disable full screen logo show |

#### 3.5.2.18 Small Logo (EPA) Show

This item allows you enabled/disabled the small EPA logo show on screen at the POST step.

| Item | Description |
|---|---|
| Enabled | EPA Logo show is enabled |
| Disabled | EPA Logo show is disabled |

### 3.5.3 Advanced Chipset Features

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.

### 3.5.3.1 DRAM Clock/Drive Control

This section can set the DRAM clock/driver timing.

| Item | Options | Description |
|---|---|---|
| DRAM Clock | By SPD<br>100NHz<br>133 MHz<br>166 MHz<br>200 MHz<br>266 MHz<br>333 MHz | Set the memory bus frequency to operate at various values for the proper memory clock setting |
| DRAM Timing | Manual<br>Auto By SPD | Set the memory timings for the said timings or DRAM Cycle Lengths of 2 or 2.5. |
| SDRAM CAS Latency [DDR/DDR2] | 1.5/2<br>2/3<br>2.5/4<br>3/5 | This controls the time dealy passing before the SDRAM starts to carry out a read command after receiving it. |
| Bank Interleave | Diabled<br>2 Bank<br>4 Bank<br>8 Bank | Enables to set the interleave mode of the SDRM interface which allows banks of SDRAM to alternate their refresh and access cycles. |
| Precharge to Active(Trp) | 2T<br>3T<br>4T<br>5T | This item sets the length of time taking to precharge a row in the memory module before a row being active and appears only when **DRAM timing** is set at **Manual**. Longer values are safer but probably not acting the best performance. |
| Active to Precharge(Tras) | 05T, 06T,07T,08T, 09T, 10T, 11T, 12T, 13T,14T, 15T, 16T, 17T, 18T, 19T, 20T | This item sets the length of time that a row staying active fore precharging and appears only when **DRAM timing** is set at **Manual**. Longer values are safer but probably not acting the best performance. |
| Active to CMD(Trcd) | 2T<br>3T<br>4T<br>5T | This timing controls the length of the delay between when a memory bank is activated to when a read/write command is sent to that bank. |
| REF to ACT/REF to REF(Trfc) | 07/08T, 08/09T… ~70T/ 71T | Set the REF to ACT/REF to REF timing.<br>This field appears when **DRAM Timing** is set at **Manual**. |
| ACT(0) to ACT(1) (TRRD) | 2T<br>3T | Set the minimum time interval between successive ACTIVE commands to the different banks. This field appears when **DRAM Timing** is set at **Manual**. |
| 1T CMD Support | Disable, Enable | Set the 1T CMD support. Rating a module as 1T is actually somewhat misleading advertising because all unbuffered modules are capable of a 1T CMD rate up to four banks per channel, beyond which chipset limitations become a factor. |

### 3.5.3.2 AGP & P2P Bridge Control

This item stores the onboard AGP and P2P function information. The reference table is as below.

| Item | Options | Description |
|---|---|---|
| AGP Aperture Size | 32M,<br>64M,<br>128M,<br>256M,<br>512M,<br>1G | Select the size of Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation. |
| AGP 2.0 Mode | 4X,<br>2X,<br>1X | This item allows you to select the AGP 2.0 mode to 4X,2X or 1X. |
| AGP Master 1 WS Write | Enabled<br>Disabled | Enabled this item to increase AGP writing |
| AGP Master 1 WS Read | Enabled<br>Disabled | Enabled this item to increase AGP reading |
| AGP 3.0 Calibration Cycle | Enabled<br>Disabled | This option allows you to disable the AGP 3.0 calibration cycle. This cycle ensures that the on-die termination impedance signal swing and slew rate of the AGP signals are calibrated on a periodic basis to ensure signal integrity.<br>It is recommended to keep this setting enabled. |
| VGA Share Memory Size | Disabled<br>64M<br>128M<br>256M | Select the size of onboard video controller's frame buffer. The buffer size are share from system memory unit. |
| Direct Frame Buffer | Enabled<br>Disabled | This item allows you to select the Direct Frame Buffer to enabled / disabled. |
| Select Display Device | CRT, LCD, CRT2,<br>DuoView, CD2,<br>CRT+LCD,<br>LCD+LCD2 | Select Display Device that the screen will be shown |
| Panel Type | 640x480 1x18B<br>800x600 1x18B<br>1024x768 1x18B<br>1280x768 1x18B<br>1280x1024 2x24B<br>1400x1050 2x18B<br>1600x1200 2x18B<br>1280x800 1x18B<br>800x480 1x18B<br>1024x768 2x18B<br>1024x768 1x24B<br>1024x768 2x24B<br>1280x768 1x24B<br>1280x1024 2x24B<br>1400x1050 2x24B<br>1600x1200 2x24B | Select Panel Resolution that will be displayed depending on the LCD Panel (LFP) |

### 3.5.3.3 CPU & PCI Bus Control

| Item | Options | Description |
|---|---|---|
| PCI Master 0 WS Write | Enabled<br>Disabled | To write PCI bus while zero wait state is executed. |
| PCI Delay Transaction | Enabled<br>Disabled | This feature is used to meet the latency of PCI cycles to and from the ISA bus. The ISA bus is much, much slower than the PCI bus. Thus, PCI cycles to and from the ISA bus take a longer time to complete and this slows the PCI bus down.<br>However, enabling **PCI Delayed Transaction** enables the chipset's embedded 32-bit posted write buffer to support delayed transaction cycles. This means that transactions to and from the ISA bus are buffered and the PCI bus can be freed to perform other transactions while the ISA transaction is underway.<br>This option should be **enabled** for better performance and to meet PCI 2.1 specifications. “Disabled” is set only if the PCI cards cannot work properly or if an ISA card that is not PCI 2.1 compliant is used. |
| VLink Mode Selection | By Auto<br>Mode 0<br>Mode 1<br>Mode 2<br>Mode 3<br>Mode 4 | The North Bridge interface to the South Bridge through a high speed(up to 1GB/Sec)8x, 66MHz Data Transfer interconnect bus caller “V-Link”. This item allows you to select the V-Link mode from 0 to 4. |
| VLink 8X Support | Enabled<br>Disabled | The feature is to toggle the V-Link bus mode between the original V-Link and the newer and faster 8X V-Link. |
| VIA PWR Management | Enabled<br>Disabled | Allows to enable VIA advanced power management. |

### 3.5.3.4 Memory Hole

You can reserve this area of system memory for ISA adapter ROM. When this area is

reserved it cannot be cached. The user information of peripherals that need to use this area of system memory usually2 discussed their memory requirements.

The choices: Disabled, 15M-16M.

#### 3.5.3.5 System BIOS Cacheable

This feature is only valid when the system BIOS is shadowed. It enables or disables the caching of the system BIOS ROM at **F0000h-FFFFFh** via the L2 cache. This greatly speeds up accesses to the system BIOS. However, this does **not** translate into better system performance because the OS does not need to access the system BIOS much.

| Item | Description |
|---|---|
| Enabled | Cacheable |
| Disabled | Non-Cacheable |

#### 3.5.3.6 Video RAM Cacheable

It enables or disables the caching of the video RAM at **A0000h-AFFFFh**. This greatly speeds up the video performance.

| Item | Description |
|---|---|
| Enabled | Cacheable |
| Disabled | Non-Cacheable |

#### 3.5.3.7 Top Performance

This item loads the BIOS settings to be optimal for the motherboard's performance.

| Item | Description |
|---|---|
| Enabled | Enable top performance |
| Disabled | Disable top performance |

### 3.5.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

```
Phoenix - AwardBIOS CMOS Setup Utility
Integrated Peripherals

▶ VIA OnChip IDE Device      [Press Enter]      Item Help
▶ VIA OnChip PCI Device      [Press Enter]
▶ SuperIO Device             [Press Enter]      Menu Level  ▶
▶ USB Device Setting         [Press Enter]

↑↓→←:Move  Enter:Select  +/-/PU/PD:Value  F10:Save  ESC:Exit  F1:General Help
   F5: Previous Values    F6: Fail-Safe Defaults    F7: Optimized Defaults
```

#### 3.5.4.1 VIA OnChip IDE Device

```
Phoenix - AwardBIOS CMOS Setup Utility
VIA OnChip IDE Device

SATA Controller            [Enabled]          Item Help
SATA Controller Mode       [RAID]
IDE DMA transfer access    [Enabled]          Menu Level  ▶
OnChip IDE Channel0        [Enabled]
OnChip IDE Channel1        [Enabled]
IDE Prefetch Mode          [Enabled]
Primary Master   PIO       [Auto]
Primary Slave    PIO       [Auto]
Secondary Master PIO       [Auto]
Primary Master   UDMA      [Auto]
Primary Slave    UDMA      [Auto]
Secondary Master UDMA      [Auto]
IDE HDD Block Mode         [Enabled]

↑↓→←:Move  Enter:Select  +/-/PU/PD:Value  F10:Save  ESC:Exit  F1:General Help
   F5: Previous Values    F6: Fail-Safe Defaults    F7: Optimized Defaults
```

| Item | Options | Description |
|---|---|---|
| SATA Controller | Enabled<br>Disabled | The chipset contains a SATA IDE interface with support for two IDE channels. Select Enabled to activate the primary IDE interface (Channel0). Select Disabled to deactivate this interface. |
| SATA Controller Mode | IDE<br>RAID<br>AHCI | Setup the onboard SATA controller mode. |
| IDE DMA Transfer Access | Enabled<br>Disabled | This BIOS feature allows you to enable or disable DMA (Direct Memory Access) support for all IDE devices |
| OnChip IDE Channel10/11 | Enabled<br>Disabled | The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary / secondary IDE interface (Channel 10/11). Select Disabled to deactivate this interface. |
| IDE Prefetch Mode | Enabled<br>Disabled | For faster drive accesses. If you install a primary and/or secondary add-in IDE interface, set this field to Disabled if the interface does not support prefetching. |
| Primary Master PIO<br>Primary Slave PIO<br>Secondary Master PIO<br>Secondary Slave PIO | Auto<br>Mode 1<br>Mode 2<br>Mode 3<br>Mode 4 | The IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device. |
| Primary Master UDMA<br>Primary Slave UDMA<br>Secondary Master UDMA<br>Secondary Slave UDMA | Auto<br>Disabled | Ultra DMA implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If the hard drive and the system software both support Ultra DMA, select Auto to enable BIOS support. |
| IDE HDD Block Mode | Enabled<br>Disabled | Block mode is also called block transfer, multiple commands, or multiple sector read/write. If the IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support. |

### 3.5.4.2 VIA OnChip PCI Device

| Item | Options | Description |
|---|---|---|
| AC97 Audio Codec | Auto<br>Disabled | This item allows you to decide to enable/disable the VIA chipset family to support AC97 Audio. |
| Lan Boot ROM | Enabled<br>Disabled | This item allows you to choose remote control Boot ROM by LAN. |

### 3.5.4.3 Super IO Device

```
                    Phoenix - AwardBIOS CMOS Setup Utility
                              SuperIO Device

   Onboard Serial Port 1      [3F8/IRQ4]          Item Help
   Onboard Serial Port 2      [2F8/IRQ3]
   Onboard Parallel Port      [378/IRQ7]          Menu Level  ►
   Parallel Port Mode         [SPP]
   EPP Mode Select            [EPP1.7]
   ECP Mode Use DMA           [3]
   Watch Dog Function         [Disabled]
 x Watch Dog Timer (Min)         1
   Onboard IR Port            [Enabled]
   Onboard IR Port Use IRQ    [IRQ5]
   Onboard Serial Port 3      [3E8]
   Serial Port 3 Use IRQ      [IRQ5]
   Onboard Serial Port 4      [2E8]
   Serial Port 4 Use IRQ      [IRQ10]

 ↑↓→←:Move  Enter:Select  +/-/PU/PD:Value  F10:Save  ESC:Exit  F1:General Help
    F5: Previous Values    F6: Fail-Safe Defaults    F7: Optimized Defaults
```

| Item | Options | Description |
|---|---|---|
| Onboard Serial Port 1<br>Onboard Serial Port 2 | Disabled<br>3F8/IRQ4<br>2F8/IRQ3<br>3E8/IRQ4<br>2E8/IRQ3<br>AUTO | Select an address and corresponding interrupt for the first and second serial ports. |
| Onboard Parallel Port | Disabled<br>378/IRQ7<br>278/IRQ5<br>3BC/IRQ7 | Select a matching address and interrupt for the physical parallel (printer) port. |
| Parallel Port Mode | SPP<br>EPP<br>ECP<br>ECP+EPP | Select an operating mode for the onboard parallel port. Select Compatible or Extended unless you are certain both your hardware and software support EPP or ECP mode. |
| EPP Mode Select | EPP1.9, EPP1.7 | Allows you to select the version of EPP that the parallel port should use. |
| ECP Mode Use DMA | 1<br>3 | Select a DMA channel for the port. |
| Watch Dog Function | Enabled<br>Disabled | This item allows you to decide enable/disable Watch Dog function |
| Watch Dog Timer | 1~255Min | This option will determine watch dog timer. |
| Onboard IR Port | Enabled<br>Disabled | This item allows you to enable onboard IR port. |
| Onboard IR Port Use IRQ | IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, RQ10, IRQ11 | Select a matching address and interrupt for onboard IR port. |
| Onboard Serial Port 3 | 3E8, 2E8, Disable | Select a matching address for onboard serial port 3. |
| Serial Port 3 Use IRQ | IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, RQ10, IRQ11 | Select a matching address and interrupt for Serial Port 3. |
| Onboard Serial Port 4 | 3E8, 2E8, Disable | Select a matching address for onboard serial port 4. |
| Serial Port 4 Use IRQ | IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, RQ10, IRQ11 | Select a matching address and interrupt for Serial Port 4. |

### 3.5.4.4 USB Device Setting

```
Phoenix - AwardBIOS CMOS Setup Utility
USB Device Setting

USB 1.0 Controller          [Enabled]
USB 2.0 Controller          [Enabled]
USB Operation Mode          [High Speed]
USB Keyboard Function       [Enabled]
USB Mouse Function          [Enabled]
USB Storage Function        [Enabled]

*** USB Mass Storage Device Boot Setting ***
UFDDA                        USB Floppy
UFDDB                        USB Floppy
No Device                   [Auto mode]
No Device                   [Auto mode]
No Device                   [Auto mode]
No Device                   [Auto mode]
No Device                   [Auto mode]
No Device                   [Auto mode]
No Device                   [Auto mode]
No Device                   [Auto mode]

Item Help

Menu Level  ▶

[Enable] or [Disable]
Universal Host
Controller
Interfacefor Universal
Serial Bus.

↑↓→←:Move  Enter:Select  +/-/PU/PD:Value  F10:Save  ESC:Exit  F1:General Help
F5: Previous Values  F6: Fail-Safe Defaults  F7: Optimized Defaults
```

| Item | Options | Description |
|---|---|---|
| USB 1.0 Controller | Enabled<br>Disabled | This item allows you to enable or disable the USB 1.0 support. |
| USB 2.0 Controller | Enabled<br>Disabled | This item allows you to enable or disable the USB 2.0 support. |
| USB Operation Mode | Full/Low Speed<br>High Speed | This item allows you to select USB operation mode. |
| USB Keyboard Function | Enabled<br>Disabled | This item allows you to enable or disable the USB keyboard support. |
| USB Mouse Function | Enabled<br>Disabled | This item allows you to enable or disable the USB mouse support. |
| USB Storage Function | Enabled<br>Disabled | This item allows you to enable or disable the USB storage support. |

### 3.5.5 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.

#### 3.5.5.1 ACPI Function

This item allows you to enable/disable the ACPI function.

The choices: Enabled, Disabled.

#### 3.5.5.2 ACPI Suspend Type

The item allows you to select the suspend type under the ACPI operating system.

The choices: S1(POS), S3(STR), S1&S3

#### 3.5.5.3 Power Management Option

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

| Item | Description |
|---|---|
| Min Saving | Minimum power management,<br>HDD Power Down = 15 Min, |
| Max Saving | Maximum power management,<br>HDD Power Down =1 Min, |
| User Define | Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr. except for HDD Power Down which ranges from 1 min. to 15 min. and disable. |

#### 3.5.5.4 HDD Power Down

There are three selections for Power Management Option; both of them have fixed mode settings.

The choices: Disable, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 Min.

#### 3.5.5.5 Suspend Mode

This setting defines the number of minutes before the system enters "suspend mode", the deepest level of system inactivity shutdown. The exact definition depends on the system, but in general this mode means that all system devices are shutdown (except for any that the BIOS is specifically told to keep running) and the processor is shut down to a trickle mode..

The choices: Disable, 1, 2, 4, 6, 8, 10, 20, 30, 40 Min, 1 Hour.

#### 3.5.5.6 Video Off Option

This determines the manner in which the monitor is always on or turned off during suspend mode.

The choices: Always On, Suspend -> Off

#### 3.5.5.7 Video Off Method

This determines the manner in which the monitor is always turned off during suspend mode.

The choices: Blank Screen, V/H SYNC+Blank, DPMS Support.

#### 3.5.5.8 MODEM Use IRQ

This determines the IRQ in which the MODEM can use.

The choices: NA, 3, 4, 5, 7, 9, 10, 11.

#### 3.5.5.9 Soft-Off by PWRBTN

Pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has "hung".(Only could working on ATX Power supply)

The choices: Delay 4 Sec, Instant-Off.

#### 3.5.5.10 Run VGABIOS if S3 Resume

Select whether to run VGA BIOS if resuming from S3 state. This is only necessary for older VGA drivers..

The choices: Auto, Yes, No.

#### 3.5.5.11 Ac Loss Auto Restart:

This item is to set whether to run Ac Loss Auto Restart.

The choices: Off, On, Former-Sts.

### 3.5.5.12 Wakeup Event Detect

| Item | Options | Description |
|---|---|---|
| PS2KB Wakeup Select | Hot Key<br>Password | This item allows you to select Hot Key or Password to wake-up the system by PS2 Keyboard. When select Password, please press ENTER key to change password max 8 numbers. |
| PS2KB Wakeup Key Select | Ctrl+F1, Ctrl+F2<br>Ctrl+F3, Ctrl+F4<br>Ctrl+F5, Ctrl+F6<br>Ctrl+F7, Ctrl+F8<br>Ctrl+F9, Ctrl+F10<br>Ctrl+F11, Ctrl+F12<br>Power, Wake, Any Key | This item allows you to set a Hot Key to wake-up the system by PS2 Keyboard.<br>Note: Power and Wake are Windows98 Keyboard button. |
| PS2MS Wakeup Key Select | Any Button<br>Left Button<br>Right Button | This item allows you to set a Hot Key to wake-up the system by PS2 mouse. |
| Wake Up On GPI | Enabled<br>Disabled | This item allows you to wake up the system via GPI. |
| PowerOn by PCI Card | By OS<br>Enabled | Enable activity detected from any PCI card to power up the system or resume from a suspended state. |
| Modem Ring Resume | BY OS<br>Enabled | This item allows the modem ring to wake up the computer system from a power saving mode. |
| RTC Alarm Resume | Enabled<br>Disabled | Sets a scheduled time and/or date to automatically power on the system. |

### 3.5.6 PnP / PCI Configuration

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.

```
                Phoenix - AwardBIOS CMOS Setup Utility
                          PnP/PCI Configurations

   PNP OS Installed            [No]          |        Item Help
   Init Display First          [PCI Slot]    |
   Reset Configuration Data    [Disabled]    | Menu Level  ▶
                                             |
   Resources Controlled By     [Auto(ESCD)]  | Select Yes if you are
 x IRQ Resources                Press Enter  | using a Plug and Play
                                             | capable operating
   PCI/VGA Palette Snoop       [Disabled]    | system Select No if
   Assign IRQ For VGA          [Enabled]     | you need the BIOS to
   Assign IRQ For USB          [Enabled]     | configure non-boot
                                             | devices
   ** PCI Express relative items **          |
   Maximum Payload Size        [4096]        |

 ↑↓→←:Move  Enter:Select  +/-/PU/PD:Value  F10:Save  ESC:Exit  F1:General Help
    F5: Previous Values    F6: Fail-Safe Defaults    F7: Optimized Defaults
```

#### 3.5.6.1 PNP OS Installed

This item allows you to determine install PnP OS or not.

The choices: Yes, No.

#### 3.5.6.2 Init Display First

Normally, you set it as PCI Slot. It means what Video Card will be initialized before the other. If you have two in your system but only one monitor, such as one AGP and one PCI, then this can effect what is displayed on the monitor..

The choices: PCI Slot, Onboard, AGP.

#### 3.5.6.3 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

The choices: Enabled, Disabled.

#### 3.5.6.4 Resources Controlled By

The Award Plug and Play BIOS has the capacity to automatically configure all of the boot

and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. If you set this field to “manual” choose specific resources by going into each of the sub menu that follows this field (a sub menu is preceded by a “➢”).
The choices: Auto(ESCD), Manual.

#### 3.5.6.5 IRQ Resource

When you set resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.
This item allows you to determine the IRQ assigned to PCI device or reserved the IRQ.
The Choices: PCI Device, Reserved.

#### 3.5.6.6 PCI / VGA Palette Snoop

Leave this field at Disabled.
The choices: Enabled, Disabled.

#### 3.5.6.7 Assign IRQ For VGA

While the system has one VGA controller and more than one VGA devices are connected, then “Enabled” is set. If the system VGA controller is not used, then “Disabled” is set.
The choices: Enabled, Disabled.

#### 3.5.6.8 Assign IRQ For USB

While the system has one USB controller and more than one USB devices are connected, then “Enabled” is set. If the system USB controller is not used, then “Disabled” is set.
The choices: Enabled, Disabled.

#### 3.5.6.9 Maximum Payload Size

This field is used to select the maximum TLP payload size of the PCI Express devices. The unit is byte.
The choices: 128, 256, 512, 1024, 2048, 4096.

### 3.5.7 PC Health Status

#### 3.5.7.1 CPU Shutdown Temp.

This section determines the shutdown temperature of your CPU.
The choices: Disabled, 75°C/167°F, 80°C/176°F, 85°C/185°F

Phoenix - AwardBIOS CMOS Setup Utility
PC Health Status
CPU Shutdown Temp. [Disabled]
Current CPU Temp
Current System Temp
CPU Fan Speed
System Fan Speed
+3.3V
+2.5V
+1.8V
CPU Vcore
Item Help
Menu Level
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

### 3.5.8 Frequency / Voltage Control

This menu specifies your setting for frequency/voltage control.

#### 3.5.8.1 CPU Clock Ratio:

This item allows you to set CPU Clock Ratio.

The choices: Min. 4X, Max. 10X.

#### 3.5.8.2 Auto Detect PCI Clk:

This item allows you to enable/disable auto detect PCI Clock.

The choices: Enabled, Disabled.

#### 3.5.8.3 Spread Spectrum

This item is to adjust extreme values of the pulse for EMI test.

The choices: Enabled, Disabled.

### 3.5.9 Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

Press <Y> to load the default values setting for optimal performance system operations.

### 3.5.10 Set Supervisor / User Password

You can set either supervisor or user password, or both of them.

Supervisor Password: able to enter/change the options of setup menus.

User Password: able to enter but no right to change the options of setup menus.

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be

asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

**PASSWORD DISABLED.**

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration. Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer. You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to "System", the password will be required both at boot and at entry to Setup. If set to "Setup", prompting only occurs when trying to enter Setup

### 3.5.11 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

Enter <Y> to store the selection made in the menus in CMOS, a special section in memory that stays on after turning the system off. The BIOS configures the system according to the Setup selection stored in CMOS when boot the computer next time.

The system is restarted after saving the values.

### 3.5.12 Exit Without Save

Abandon all CMOS value changes and exit setup, and the system is restarted after exiting.

# 4 Drivers Installation

**Note**: Installation procedures and screen shots in this section are for your reference and may not be exactly the same as shown on your screen.

## 4.1 Install Chipset Driver (For VIA CN896)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Chipset\VIA\CN896.**

**Note:** The installation procedures and screen shots in this section are based on Windows XP operation system.

**Step 1.** Locate「\Driver_Audio\VIA\CN896\VIA_HyperionPro_V513A\setup.exe」.

**Step 2.** Click **Next**.

**Step 3.** Select **I Agree** and click **Next** to the following step.

**Step 4.** Select both items and click **Next** to run the setup.

**Step 5.** Click **Next**.

**Step 6.** Click **Next**.

**Step 7.** Click Finish to restart the PC.

## 4.2 Install Display Driver (For VIA CN896)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **Driver_Display\VIA\CN896**.

**Note:** The installation procedures and screen shots in this section are based on Windows XP operation system.

**Step1.** Locate \Drivers\Driver_Video\VIA\CN896\VN896(CE)_200001i_XP_wIShld_logod\wIShld\Setup.exe 」.

**Step 2.** Setup will run the installation automatically, then click **Finish** to complete.

## 4.3 Install Audio Driver (For VIA VT1616)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Audio\VIA\VT1616.**

**Note:** The installation procedures and screen shots in this section are based on Windows XP operation system.

**Step 1.** Locate「\Driver_Audio\VIA\VT1616 \A1u590b\setup.exe」.

**Step 2.** Click **Next**.

**Step 3.** Select **Install Driver** and click **Next** to the following step.

**Step 4.** Click **Continue Anyway** to run the setup.

**Step 5.** Click **Finish** to complete the setup and restart the PC.

## 4.4 Install Ethernet Driver (For Realtek RTL8101E)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **D:\Driver_Gigabit\Realtek\ RTL8101E**.

**Note:** The installation procedures and screen shots in this section are based on Windows XP operation system.

**Step 1.** Locate 「\Driver_Gigabit\Realtek\ RTL8101E\PCIE_Install_5678(installshield 12_1.13)_1011\Setup.exe」.

**Step 2.** Click **Next**.

**Step 3.** Click **Next** to run the installation.

**Step 4.** Click **Finish** to complete the setup.

# 5 Mechanical Drawing

## EBM-CN896 Series

**(Unit: mm)**

# Appendix A: BIOS Revisions

**BIOS Rev.**

**New Features**

**Bugs/Problems Solved**

**Known Problems**

# Appendix B: AWARD BIOS POST Messages

## Overview

During the Power On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

## Post Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

## Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and the EISA BIOS.

**1. CMOS BATTERY HAS FAILED**

CMOS battery is no longer functional. It should be replaced.

**2. CMOS CHECKSUM ERROR**

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

**3. DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER**

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

**4. DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP**

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

**5. DISPLAY SWITCH IS SET INCORRECTLY**

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

**6. DISPLAY TYPE HAS CHANGED SINCE LAST BOOT**

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

**7. EISA Configuration Checksum Error**

**PLEASE RUN EISA CONFIGURATION UTILITY**

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the card is installed firmly in the slot.

**8. EISA Configuration Is Not Complete**

**PLEASE RUN EISA CONFIGURATION UTILITY**

The slot configuration information stored in the EISA non-volatile memory is incomplete.

**Note:** When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

**9. ERROR ENCOUNTERED INITIALIZING HARD DRIVE**

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

**10. ERROR INITIALIZING HARD DISK CONTROLLER**

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

**11. FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT**

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

**12. Invalid EISA Configuration**

**PLEASE RUN EISA CONFIGURATION UTILITY**

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.

**Note:** When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

**13. KEYBOARD ERROR OR NO KEYBOARD PRESENT**

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

**14. Memory Address Error at ...**

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

**15. Memory parity Error at ...**

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

**16. MEMORY SIZE HAS CHANGED SINCE LAST BOOT**

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

**17. Memory Verify Error at ...**

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

**18. OFFENDING ADDRESS NOT FOUND**

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

**19. OFFENDING SEGMENT:**

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

**20. PRESS A KEY TO REBOOT**

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

**21. PRESS F1 TO DISABLE NMI, F2 TO REBOOT**

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

**22. RAM PARITY ERROR - CHECKING FOR SEGMENT ...**

Indicates a parity error in Random Access Memory.

**23. Should Be Empty But EISA Board Found**

**PLEASE RUN EISA CONFIGURATION UTILITY**

A valid board ID was found in a slot that was configured as having no board ID.

**Note:** When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

**24. Should Have EISA Board But Not Found**

**PLEASE RUN EISA CONFIGURATION UTILITY**

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

**Note:** When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

**25. Slot Not Empty**

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

**Note:** When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

**26. SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT ...**

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

**27. Wrong Board In Slot**

**PLEASE RUN EISA CONFIGURATION UTILITY**

The board ID does not match the ID stored in the EISA non-volatile memory.

**Note:** When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

**28. FLOPPY DISK(S) fail (80) → Unable to reset floppy subsystem.**

**29. FLOPPY DISK(S) fail (40) → Floppy Type dismatch.**

**30. Hard Disk(s) fail (80) → HDD reset failed.**

**31. Hard Disk(s) fail (40) → HDD controller diagnostics failed.**

**32. Hard Disk(s) fail (20) → HDD initialization error.**

**33. Hard Disk(s) fail (10) → Unable to recalibrate fixed disk.**

**34. Hard Disk(s) fail (08) → Sector Verify failed.**

**35. Keyboard is locked out - Unlock the key.**

BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

**36. Keyboard error or no keyboard present.**

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

**37. Manufacturing POST loop.**

System will repeat POST procedure infinitely while the P15 of keyboard controller is pull low. This is also used for M/B burn in test.

**38. BIOS ROM checksum error - System halted.**

The checksum of ROM address F0000H-FFFFFH is bad.

**39. Memory test fail.**

BIOS reports the memory test fail if the onboard memory is tested error.

## 40. POST Codes

| POST (hex) | Description |
|---|---|
| CFh | Test CMOS R/W functionality. |
| C0h | Early chipset initialization:<br>-Disable shadow RAM<br>-Disable L2 cache (socket 7 or below)<br>-Program basic chipset registers |
| C1h | Detect memory<br>-Auto-detection of DRAM size, type and ECC.<br>-Auto-detection of L2 cache (socket 7 or below) |
| C3h | Expand compressed BIOS code to DRAM |
| C5h | Call chipset hook to copy BIOS back to E000 & F000 shadow RAM. |
| 0h1 | Expand the Xgroup codes locating in physical address 1000:0 |
| 02h | Reserved |
| 03h | Initial Superio_Early_Init switch. |
| 04h | Reserved |
| 05h | 1. Blank out screen<br>2. Clear CMOS error flag |
| 06h | Reserved |
| 07h | 1. Clear 8042 interface<br>2. Initialize 8042 self-test |
| 08h | 1. Test special keyboard controller for Winbond 977 series Super I/O chips.<br>2. Enable keyboard interface. |
| 09h | Reserved |
| 0Ah | 1. Disable PS/2 mouse interface (optional).<br>2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional).<br>3. Reset keyboard for Winbond 977 series Super I/O chips. |
| 0Bh | Reserved |
| 0Ch | Reserved |
| 0Dh | Reserved |
| 0Eh | Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker. |
| 0Fh | Reserved |
| 10h | Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support. |
| 11h | Reserved |
| 12h | Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override. |
| 13h | Reserved |
| 14h | Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers. |

| POST (hex) | Description |
|---|---|
| 15h | Reserved |
| 16h | Initial Early_Init_Onboard_Generator switch. |
| 17h | Reserved |
| 18h | Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686). |
| 19h | Reserved |
| 1Ah | Reserved |
| 1Bh | Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR. |
| 1Ch | Reserved |
| 1Dh | Initial EARLY_PM_INIT switch. |
| 1Eh | Reserved |
| 1Fh | Load keyboard matrix (notebook platform) |
| 20h | Reserved |
| 21h | HPM initialization (notebook platform) |
| 22h | Reserved |
| 23h | 1. Check validity of RTC value:<br>e.g. a value of 5Ah is an invalid value for RTC minute.<br>2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead.<br>3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information.<br>4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots.<br>5. Early PCI initialization:<br>-Enumerate PCI bus number<br>-Assign memory & I/O resource<br>-Search for a valid VGA device & VGA BIOS, and put it into C000:0. |
| 24h | Reserved |
| 25h | Reserved |
| 26h | Reserved |
| 27h | Initialize INT 09 buffer |
| 28h | Reserved |
| 29h | 1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address.<br>2. Initialize the APIC for Pentium class CPU.<br>3. Program early chipset according to CMOS setup. Example: onboard IDE controller.<br>4. Measure CPU speed.<br>5. Invoke video BIOS. |
| 2Ah | Reserved |
| 2Bh | Reserved |
| 2Ch | Reserved |

| POST (hex) | Description |
|---|---|
| 2Dh | 1. Initialize multi-language<br>1. Put information on screen display, including Award title, CPU type, CPU speed …. |
| 2Eh | Reserved |
| 2Fh | Reserved |
| 30h | Reserved |
| 31h | Reserved |
| 32h | Reserved |
| 33h | Reset keyboard except Winbond 977 series Super I/O chips. |
| 34h | Reserved |
| 35h | Reserved |
| 36h | Reserved |
| 37h | Reserved |
| 38h | Reserved |
| 39h | Reserved |
| 3Ah | Reserved |
| 3Bh | Reserved |
| 3Ch | Test 8254 |
| 3Dh | Reserved |
| 3Eh | Test 8259 interrupt mask bits for channel 1. |
| 3Fh | Reserved |
| 40h | Test 8259 interrupt mask bits for channel 2. |
| 41h | Reserved |
| 42h | Reserved |
| 43h | Test 8259 functionality. |
| 44h | Reserved |
| 45h | Reserved |
| 46h | Reserved |
| 47h | Initialize EISA slot |
| 48h | Reserved |
| 49h | 1. Calculate total memory by testing the last double word of each 64K page.<br>2. Program writes allocation for AMD K5 CPU. |
| 4Ah | Reserved |
| 4Bh | Reserved |
| 4Ch | Reserved |
| 4Dh | Reserved |
| 4Eh | 1. Program MTRR of M1 CPU<br>2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range.<br>3. Initialize the APIC for P6 class CPU.<br>4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical. |
| 4Fh | Reserved |
| 50h | Initialize USB |

| POST (hex) | Description |
|---|---|
| 51h | Reserved |
| 52h | Test all memory (clear all extended memory to 0) |
| 53h | Reserved |
| 54h | Reserved |
| 55h | Display number of processors (multi-processor platform) |
| 56h | Reserved |
| 57h | 1. Display PnP logo<br>2. Early ISA PnP initialization<br>-Assign CSN to every ISA PnP device. |
| 58h | Reserved |
| 59h | Initialize the combined Trend Anti-Virus code. |
| 5Ah | Reserved |
| 5Bh | (Optional Feature)<br>Show message for entering AWDFLASH.EXE from FDD (optional) |
| 5Ch | Reserved |
| 5Dh | 1. Initialize Init_Onboard_Super_IO switch.<br>2. Initialize Init_Onbaord_AUDIO switch. |
| 5Eh | Reserved |
| 5Fh | Reserved |
| 60h | Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility. |
| 61h | Reserved |
| 62h | Reserved |
| 63h | Reserved |
| 64h | Reserved |
| 65h | Initialize PS/2 Mouse |
| 66h | Reserved |
| 67h | Prepare memory size information for function call:<br>INT 15h ax=E820h |
| 68h | Reserved |
| 69h | Turn on L2 cache |
| 6Ah | Reserved |
| 6Bh | Program chipset registers according to items described in Setup & Auto-configuration table. |
| 6Ch | Reserved |
| 6Dh | 1. Assign resources to all ISA PnP devices.<br>2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO". |
| 6Eh | Reserved |
| 6Fh | 1. Initialize floppy controller<br>2. Set up floppy related fields in 40:hardware. |
| 70h | Reserved |
| 71h | Reserved |
| 72h | Reserved |

| POST (hex) | Description |
|---|---|
| 73h | (Optional Feature)<br>Enter AWDFLASH.EXE if :<br>-AWDFLASH is found in floppy drive.<br>-ALT+F2 is pressed |
| 74h | Reserved |
| 75h | Detect & install all IDE devices: HDD, LS120, ZIP, CDROM….. |
| 76h | Reserved |
| 77h | Detect serial ports & parallel ports. |
| 78h | Reserved |
| 79h | Reserved |
| 7Ah | Detect & install co-processor |
| 7Bh | Reserved |
| 7Ch | Reserved |
| 7Dh | Reserved |
| 7Eh | Reserved |
| 7Fh | 1. Switch back to text mode if full screen logo is supported.<br>-If errors occur, report errors & wait for keys<br>-If no errors occur or F1 key is pressed to continue:<br>◆Clear EPA or customization logo. |
| 80h | Reserved |
| 81h | Reserved |
| 82h | 1. Call chipset power management hook.<br>2. Recover the text fond used by EPA logo (not for full screen logo)<br>3. If password is set, ask for password. |
| 83h | Save all data in stack back to CMOS |
| 84h | Initialize ISA PnP boot devices |
| 85h | 1. USB final Initialization<br>2. NET PC: Build SYSID structure<br>3. Switch screen back to text mode<br>4. Set up ACPI table at top of memory.<br>5. Invoke ISA adapter ROMs<br>6. Assign IRQs to PCI devices<br>7. Initialize APM<br>8. Clear noise of IRQs. |
| 86h | Reserved |
| 87h | Reserved |
| 88h | Reserved |
| 89h | Reserved |
| 90h | Reserved |
| 91h | Reserved |
| 92h | Reserved |
| 93h | Read HDD boot sector information for Trend Anti-Virus code |

| POST (hex) | Description |
|---|---|
| 94h | 1. Enable L2 cache<br>1. Program boot up speed<br>2. Chipset final initialization.<br>3. Power management final initialization<br>4. Clear screen & display summary table<br>5. Program K6 write allocation<br>6. Program P6 class write combining |
| 95h | 1. Program daylight saving<br>1. Update keyboard LED & typematic rate |
| 96h | 1. Build MP table<br>2. Build & update ESCD<br>3. Set CMOS century to 20h or 19h<br>4. Load CMOS time into DOS timer tick<br>5. Build MSIRQ routing table. |
| FFh | Boot attempt (INT 19h) |