

User's Manual

ECB-641 / ECB-641C

**STPC Elite / Consumer II 133 Half-size CPU Card with LCD Interface,
10/100Base-Tx Ethernet**

1st Ed. – 06 April, 2005

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5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 ECB-641 STPC Elite / ECB-641C Consumer II 133 Half-size CPU card
- 1 Quick Installation Guide
- 1 CD-ROM or DVD-ROM contains the followings:
 - User's Manual (this manual in PDF file)
 - Ethernet driver and utilities
 - VGA drivers and utilities
- Cable set includes the followings:
 - 1 ATA-33 IDE cable (40-pin, pitch 2.54mm)
 - 1 FDD cable (34-pin, pitch 2.54mm)
 - 1 Bracket with one Serial and one Printer cable (10-pin 2.54mm / 26-pin 2.54mm)
 - 1 PS/2 keyboard and mouse Y cable (6-pin, Mini-DIN)

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

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Document Amendment History

Revision	Date	By	Comment
1 st	Apr. '05.	Scott Tseng	Initial Release

1. Manual Objectives

This manual describes in detail the Evaluate Technology ECB-641 Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with ECB-641 or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

2. Introduction

2.1 System Overview

The ECB-641 / 641C is an ISA half-size Single Board Computer that equips with STPC Elite / Consumer II processor, LCD interface, PCI-bus Ethernet interface, and 32 / 64 MB SDRAM onboard.

Targeting on the rapid growing networking and embedded system markets, the ECB-641 integrates a PCI-bus Realtek RTL8100B 10/100Base-Tx Ethernet controller. Running on the STPC Elite / Consumer II 133MHz Low Power CPU and SMI 712 chipset, the ECB-641 is also ideal for the demanding Internet Access Devices or Mobile Applications that require a low-power and low-heat dissipation Single Board Computer, such as WBT (Windows Based Terminal), Thin Client, STB (Set Top Box), Web Phone, and other Information Appliances.

Other impressive features include a built-in 40-pin TFT LCD interface, a 32-pin M-Systems DiskOnChip socket supports Flash memory capacity from 8MB to 1 GB, a Compact Flash card connector, two serial ports, one parallel port, and a 144-pin SODIMM socket allowing for up to 64MB of SDRAM to be installed.

2.2 System Specifications

General Functions

- **Bus interface:** ISA bus
- **CPU:** Onboard STPC Elite / Consumer II 133MHz, BGA package
- **BIOS:** Award 256KB Flash BIOS.
- **Chipset:** STPC Elite / Consumer II 133
- **I/O Chipset:** Winbond W83977F-A
- **Memory:** Onboard 32 / 64 Mbytes and one 144-pin SODIMM socket supports up to 128MB SDRAM
- **Enhanced IDE:** Supports up to four IDE devices. Supports PIO Mode 4 with data transfer rate up to 14MB/sec. (20 x 2, pitch 2.54mm header for Primary IDE and 22 x 2, pitch 2.0mm header for Secondary IDE)
- **FDD Interface:** Supports up to two floppy disk drives, 5.25" (360KB and 1.2MB) and/or 3.5" (720KB, 1.44MB, and 2.88MB)
- **Parallel Port:** Internal header for bi-directional parallel port x 1. Supports SPP, ECP, and EPP modes. (13 x 2, pitch 2.54mm header)
- **Serial Port:** One RS-232 and one RS-232/422/485 serial port. Ports can be configured as COM1, COM2 or disabled individually. (16C550 equivalent)
- **IR Interface:** Supports one IrDA Tx/Rx header
- **KB/Mouse Connector:** One 6-pin mini-DIN connector supports PS/2 keyboard and mouse
- **Watchdog Timer:** Can generate a system reset. Software selectable time-out interval (16 sec. ~ 127min., 30 sec./step)
- **Power Management:** Supports AT / ATX power supply.

Flat Panel/CRT Interface

- **Chipset:** SMI LynxEM +SM712, high performance 64-bit GUI, 2D engine
- **Display Memory:** 2MB SDRAM frame buffer on LynxEM +SM712
- **Display Type:** Supports CRT and flat panel (TFT and Color DSTN) displays
- **Resolution:** Up to 1024 x 768, 1280 x 1024 (641C)

Ethernet Interface

- **Chipset:** Realtek RTL8100B PCI-bus Ethernet controllers onboard
- **Ethernet Interface:** PCI 100/10 Mbps, IEEE 802.3U compatible

SSD Interface

One 32-pin DIP socket supports M-Systems DiskOnChip 2000 series, memory capacity from 8MB to 1GB

One CF socket supports Type I / II Compact Flash Card

Digital I/O Interface

4-bit TTL digital input & 4-bit TTL digital output

Expansion Interface

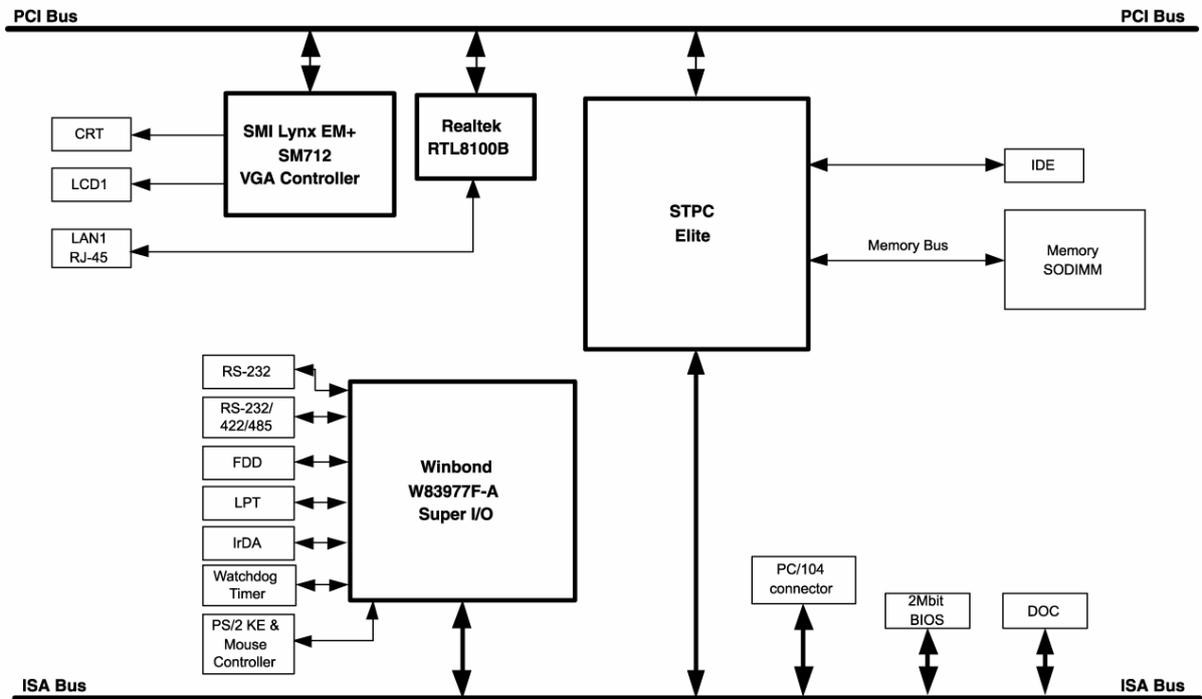
- **PC/104 Connectors:** One 16-bit 104-pin connector onboard

Mechanical and Environmental

- **Power Supply Voltage:** +5V (4.75V to 5.25V), 12V (11.4V to 12.6V)
- **Typical Power Requirement:** 5V
- **Operating Temperature:** 32 to 140 °F (0 to 60 °C)
- **Board Size:** 7.3" (L) x 4.8" (W) (185mm x 122mm)
- **Weight:** 0.4 Kg

2.3 Architecture Overview

The following block diagram shows the architecture and main components of ECB-641 series.



The following sections provide detail information about the functions provided onboard.

2.3.1 STPC Elite

The STPC Elite integrates a fully static x86 processor up to 133MHz, fully compatible with standard x86 processors, and combines it with powerful chipset to provide a general purpose PC compatible subsystem on a single device. The device is packaged in a 388 Ball Grid Array (PBGA).

- Powerful x86 processor
- 64-bit SDRAM controller at 100MHz
- Integrated PCI North / South Bridge controller
- ISA Master / Slave / DMA
- 16-bit local bus interface for low cost and embedded applications
- EIDE controller
- Integrated peripheral controller – DMA controller / Interrupt controller / Timer / counters
- Power management unit
- IC Interface
- 16 enhanced general purpose I/Os
- JTAG IEEE 1149.1
- Programmable output clock up to 135 MHz
- Commercial and Industrial temperature ranges

2.3.2 STPC Consumer II

The STPC Elite integrates a standard 5th generation x86 core, a Synchronous DRAM controller, a graphic subsystem, a video pipeline, and support logic including PCI, ISA, and IDE controllers to provide a single consumer orientated PC compatible subsystem on a single device. The device is based on a tightly coupled Unified Memory Architecture (UMA), sharing memory between the CPU, the graphics and the video. The STPC consumer II is packaged in a 388 Plastic Ball Grid Array (PBGA).

- Powerful x86 processor
- 64-bit SDRAM UMA controller
- VGA & SVGA CRT controller
- 135MHz RAMDAC
- 2D graphics engine
- Video Input Port
- Video Pipeline – up-scaler / video color space converter / chroma & color key support
- TV Output – three-line flicker filter / ITU-R 601/656 scan converter / NTSC / PAL composite, RGB, S-video
- ISA Master / Slave
- Optional 16-bit local bus interface
- EIDE controller
- IC Interface
- IPC – DMA controller / Interrupt controller / Timer / counters
- Power Management Unit
- JTAG IEEE 1149.1

2.3.3 SMI LynxEM+ SM712 VGA Controller

The LynxEM+ consists of a logic block which interfaces to a 2MB block of internal memory. The internal memory configuration consists of one 512Kx32 SGRAM, and supports single clock cycle transfers up to 125MHz. Peak memory bandwidth for the internal memory bus is over 500MB/s. The logic within the LynxEM+ consists of 11 functional blocks: PCI Interface, Host Interface (HIF), Memory Controller, Drawing Engine, Power Down Control Unit, Video Processor, Video Capture Module, LCD Backend Controller, VGA Core, PLL Module, and RAMDAC. A summary of each of the functional blocks, along with important features follows:

- Frame based 66 MHz AGP support
- 33 MHz PCI Master/Slave interface
- PCI 2.1 compliant
- Dual aperture feature for concurrent VGA and video/drawing engine access
- 500MB/s memory bandwidth
- Dynamic Power Management
- Virtual Refresh
- Multiple video windows in HW
- Independent video sources on different displays
- Bi-linear scaling
- TFT and DSTN support up to 1280x1024
- Timing generation for Virtual Refresh
- EMI reduction circuit
- Closed captioning function
- Popup icon location flexible
- Transparency color support
- 100% IBM VGA compatible
- Separate PLL for LCD panel timing
- RAMDAC supports pixel clock frequencies up to 135MHz at 3.3V

2.3.4 Panel Interface

An alternative display to the standard CRT monitor is digital flat panel interface in which the color of each pixel is digitally encoded. The panel data may be transferred in parallel where the color of each pixel is transferred over a number of signal lines at rates up to 80MHz.

The LynxEM+ LCD Backend Controller module manages data flow and generates timing to the selected LCD display. The module provides support for 3,9,12,18,24,36-bit TFT and 16 or 24-bit DSTN panels up to 1280x1024 resolution. The backend controller contains a color encoder, dithering engines for TFT and DSTN panels, frame accelerator, and a Virtual Refresh timing generation block. Each of the blocks within the LCD Backend controller module can be powered down if not in use. In addition LynxEM+ integrates innovative circuitry for reducing EMI.

The parallel interface is only suitable for short distance (less than 50 cm) and is typically implemented by using of ribbon cables. One should be careful in the EMC design of the box and cabling when this interface is used.

It should also be noted that the signal level of this interface is 3.3V, but does comply with the TTL signal levels. Some - most older displays require 5V signal level.

2.3.5 SDRAM Interface

This board uses SDRAM in the 144-pin DIMM form factor. 3.3V PC 100 SDRAM modules are recommended to be used.

- 64-bit data bus
- Up to 100 MHz SDRAM clock speed
- Integrated system memory, graphic frame memory and video frame memory
- Supports 2 MB up to 128 MB system memory
- Supports 16-, 64-, and 128-Mbit SDRAM
- Supports 8, 16, 32, 64, and 128 MB DIMMs
- Supports buffered, non buffered, and registered DIMMs
- Four-line write buffers for CPU to SDRAM and PCI to SDRAM cycles
- Four-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for SDRAM parameters
- Supports -8, -10, -12, -13, -15 memory parts
- Supports memory hole between 1 MB and 8 MB for PCI/ISA busses

2.3.6 IDE Interface

- Dedicated IDE pins, concurrent with PCI bus
- 4x32 bits Read-Ahead buffer and Write-Post buffer support
- Supports through ATA PIO mode 3, 4 hard disk drives

2.3.7 Realtek RTL8100B Ethernet Controller

The Realtek RTL8100B is one of the Realtek RTL8139A/B/C/8130 family, the highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that is capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management.

2.3.8 Winbond W83977F-A

The Winbond W83977F-A Super I/O chip provides most input / output interfaces of the system as the following:

- COM 1/COM 2. Operates in RS-232 mode through a charge pump driver. Only 5V supply is required
- LPT. Support for SPP, EPP and ECP modes
- Floppy interface
- Keyboard interface
- PS/2 Mouse interface
- IrDA interface for infrared communication. This interface shares the controller of COM2
- Provision of buffered ISA data bus for BIOS (denoted *XDBus*)
- ACPI Controller/Extender that supports the requirements of the ACPI spec (rev 1.0)
- An APC that controls the main power supply to the system using open-drain output
- Watchdog timer

2.3.9 M-Systems DiskOnChip Socket

M-Systems *DiskOnChip 2000* is a high performance flash disk in a standard 32-pin DIP package. This unique data storage solution offers cost effective data storage beyond that of traditional hard disks. Perfect for applications with limited space and varying capacity requirements. The *DiskOnChip 2000* is simply integrated into your CPU board and you have a bootable flash disk.

The *DiskOnChip 2000* includes M-Systems proprietary TrueFFS® (True Flash File System) technology built-in, providing complete read/write capability and hard disk emulation. TrueFFS provides hard disk compatibility at both the sector and file level. The *DiskOnChip 2000* works in all major operating systems including DOS, Windows Embedded NT/CE/2000, Linux, pSOS+, VxWorks, QNX, BE and more. It is also relatively easy to customize to work in O/S-less and non-x86 environments.

The use of TrueFFS, in conjunction with the built-in EDC/ECC, provides maximum data reliability, even under harsh operating conditions such as power failures. Advanced wear leveling ensures long flash life for maximum usage.

3. Hardware Configuration

3.1 Installation Procedure

1. Turn off the power supply.
2. Insert the SODIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the PWR1 or plug the board to passive backplane.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the "LOAD BIOS DEFAULTS" feature. The **Integrated Peripheral Setup** and the **Standard CMOS Setup** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilised, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

3.2 Safety Precautions

3.2.1 Warning!



Always completely disconnect the power cord from your chassis or power cable from your board whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

3.2.2 Caution!



Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

3.3 Installing DRAM (SODIMMs)

3.3.1 System Memory

The reverse side of the ECB-641 contains a socket for 144-pin dual inline memory module (SODIMM). The socket uses 3.3 V unbuffered synchronous DRAM (SDRAM). SODIMM module is available in capacities of 32 or 64 MB. The socket can be filled in the SODIMM of any size, giving your ECB-641 single board between 32 and 128 MB of memory.

3.3.2 Supplementary Information About DIMM

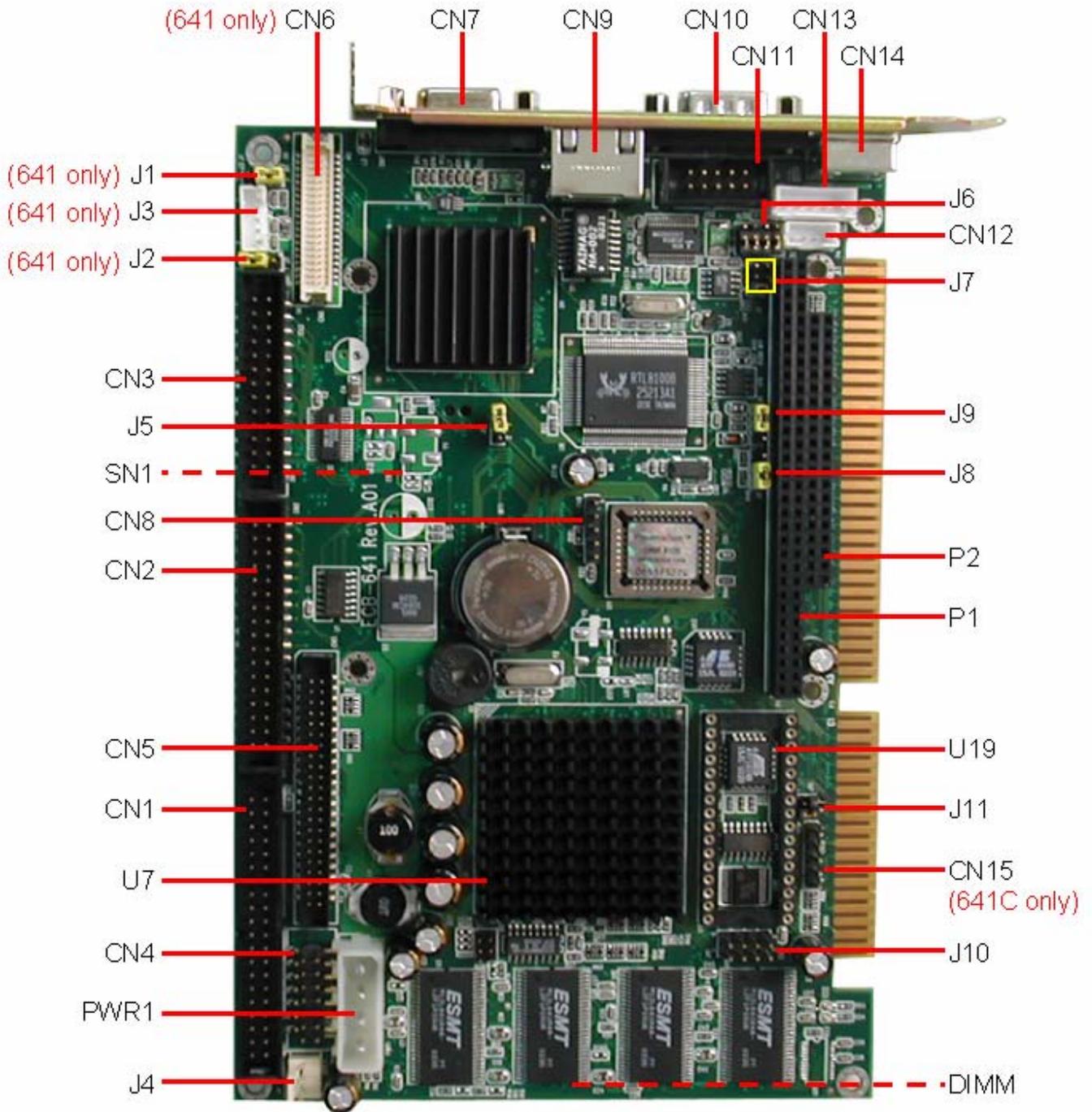
Your ECB-641 accepts both regular and PC-100 SDRAM SODIMM Module (without parity). Single-sided modules are typically 64 MB; double-sided modules are usually 32 or 128 MB.

3.3.3 Memory Installation Procedures

Press the SODIMM module right down into the socket, until you hear a click. This is when the two handles have automatically locked the memory module into the correct position of the SODIMM socket. (See Figure below) To take away the memory module, just push both handles outward, and the memory module will be ejected by the mechanism in the socket.

3.4 Jumper & Connector

3.4.1 Jumper & Connector Layout



3.4.2 Jumper & Connector List

Connectors on the board are linked to external devices such as hard disk drives, keyboard, mouse, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

The following tables list the function of each of the board's jumpers and connectors.

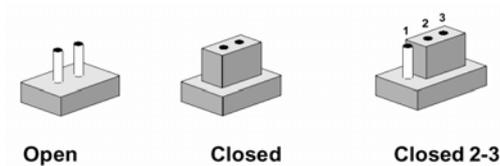
Jumpers		
Label	Function	Note
J5	CF Master/Slave mode select	2 x 1 header, pitch 2.54mm
J6	COM2 RS-232/422/485 select	4 x 3 header, pitch 2.0mm
J7	COM2 RS-232/422/485 select	3 x 2 header, pitch 2.0mm
J8	AT/ATX power select	3 x 1 header, pitch 2.54mm
J9	Clear CMOS	3 x 1 header, pitch 2.54mm
J11	M-Systems DiskOnChip memory address select	2 x 2 header, pitch 2.0mm

Connectors		
Label	Function	Note
CN1	Primary IDE connector	20 x 2 header, pitch 2.54mm
CN2	Floppy connector	17 x 2 header, pitch 2.54mm
CN3	Parallel port connector	13 x 2 header, pitch 2.54mm
CN4	Front panel connector	7 x 2 header, pitch 2.54mm
CN5	Secondary IDE connector	22 x 2 header, pitch 2.0mm
CN6	LCD panel connector (ECB-641 only)	HIROSE DF13-40DP-1.25V
CN7	VGA connector	15-pin female D-sub connector
CN8	IrDA connector	5 x 1 header, pitch 2.54mm
CN9	10/100 Base-Tx Ethernet connector	RJ-45
CN10	Serial port 1 connector	9-pin male D-sub connector
CN11	Serial port 2 connector	5 x 2 header, pitch 2.54mm
CN12	Auxiliary power connector	4 x 1 wafer, pitch 2.0mm
CN13	Internal keyboard connector	5 x 1 wafer, pitch 2.54mm
CN14	PS/2 keyboard and mouse connector	6-pin mini DIN
CN15	TV Output connector (ECB-641C only)	5-pin header, pitch 2.54mm
DIMM	144-pin SODIMM socket	
J1	LCD backlight brightness adjustment connector (ECB-641 only)	3 x 1 header, pitch 2.54mm
J2	LCD backlight contrast adjustment connector (ECB-641 only)	3 x 1 header, pitch 2.54mm
J3	LCD inverter connector (ECB-641 only)	5 x 1 wafer, pitch 2.54mm
J4	Power connector	3 x 1 wafer, pitch 2.54mm
J10	Digital I/O connector	4 x 2 header, pitch 2.54mm
P1, P2	PC/104 connector	
SN1	Compact Flash connector	
U19	M-Systems DiskOnChip socket	

3.5 Setting Jumpers

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:



A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

3.6 Setting Jumpers

3.6.1 CF Master / Slave Select (J5)

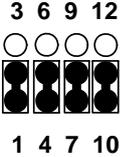
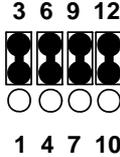
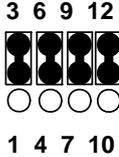
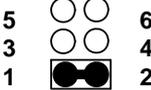
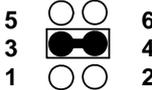
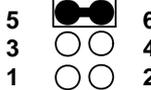
You can use J5 to short or open pin 1-2 to set Master / Slave mode for the Compact Flash.

CF Master/Slave mode Select (J5)		
	Master	Slave*
J5		

*default

3.6.2 COM2 RS-232/422/485 Select (J6, J7)

The ECB-641 COM2 serial port can be selected as RS-232, RS-422, or RS-485 by setting J6 & J7.

COM2 RS-232/422/485 Select (J6, J7)			
	RS-232*	RS-422	RS-485
J6			
J7			

*default

3.6.3 AT/ATX Power Select (J8)

You can use J8 to select the power supply type. To use the AT power supply, set the J8 to 1-2 closed. Set J8 to 2-3 closed if ATX power supply is used.

AT/ATX Power Select (J8)		
	AT P/S*	ATX P/S
J8	3 ○ 2 ● 1 ●	3 ● 2 ● 1 ○

*default

Note:

Set J4 to 2-3 closed if AT power supply is used.

3.6.4 Clear CMOS (J9)

You can use J9 to clear the CMOS data if necessary. To reset the CMOS data, set J9 to 1-2 closed for just a few seconds, and then move the jumper back to 2-3 closed.

Clear CMOS (J9)		
	Protect*	Clear CMOS
J9	3 ● 2 ● 1 ○	3 ○ 2 ● 1 ●

* default

3.6.5 M-Systems DiskOnChip Memory Address Select (J11)

The M-systems DiskOnChip memory address can be selected by J11. The choice is D0000~D1FFF, D4000~D5FFF, D8000~D9FFF, or Disabled.

M-systems DiskOnChip Memory Address Select (J11)												
	D0000*		D4000		D8000		Disabled					
J11	1 ○	2 ○	1 ●	2 ●	1 ○	2 ○	1 ●	2 ●	3 ○	4 ○	3 ●	4 ●
	3 ●	4 ●	3 ○	4 ○	4 ○	3 ○	4 ○	3 ○	4 ○	4 ●	3 ●	4 ●

* default

3.7 Connector Definitions

3.7.1 Primary IDE Connector (CN1)

Signal	PIN		Signal
RESET#	1	2	GND
D7	3	4	D8
D6	5	6	D9
D5	7	8	D10
D4	9	10	D11
D3	11	12	D12
D2	13	14	D13
D1	15	16	D14
D0	17	18	D15
GND	19	20	DCS#3
DCS2#	21	22	GND
IOW#	23	24	GND
IOR#	25	26	GND
IRDY	27	28	IRQ15
NC	29	30	GND
IRQ14	31	32	DCS#16
DA1	33	34	NC
DA0	35	36	DA2
DCS0#	37	38	DCS1#
DACT#	39	40	GND

3.7.2 Signal Description – Primary IDE Connector (CN1)

The IDE interface supports PIO modes 0 to 4.

DA [2:0]	IDE Address Bits. These are normally outputs to the ATA connector for register selection in the drives.
DCS [0:3]#	IDE Chip Selects. These are active low outputs which are used to select control/command block registers in the drives.
DCS16#	IDE Chip Select 16. This is an active-low input which indicates that the disk drive is ready to perform a 16-bit data transfer. The signal connects directly to the ATA connector and is typically driven active during IDE controller transfers to the drive's 1F0h data port. Note that an external 1K-Ohm pull-up resistor is recommended for this signal.
D [15:0]	These are the 16-bit data bus which connects to the IDE drives. D [7:0] define the lowest data byte while D [15:8] define the most significant data byte. The HDD bus is normally in a high-impedance state and is driven by the M1489 only during the HDIOWJ command pulse.
IOR#	IDE I/O Read. This is an active low output which enables data to be read from the IDE drive.
IOW#	IDE I/O Write. This is an active low output which enables data to be written to the IDE drive.
IORDY	This is an input which is sampled at the clock rising edge at the programmed end of the command cycle. If IORDYJ is sampled high, the command is terminated. If it is sampled low the command cycle is extended. IORDYJ will be sampled with every positive CLK edge until it is tested high. Once sampled high, the command will end normally. Note that an external 1K-Ohm pull-up resistor is recommended for this signal.
RESET#	IDE Reset. This signal resets all the devices that are attached to the IDE interface.
IRQ14	Interrupt line from hard disk. Connected directly to PC-AT bus.
IRQ15	Interrupt line from hard disk. Connected directly to PC-AT bus.
DACT#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low.

3.7.3 Floppy Connector (CN2)

Signal	PIN		Signal
GND	1	2	DRV DEN0#
GND	3	4	NC
GND	5	6	DRV DEN1#
GND	7	8	INDEX#
GND	9	10	MOA#
GND	11	12	DSB#
GND	13	14	DSA#
GND	15	16	MOB#
GND	17	18	DIR#
GND	19	20	STEP#
GND	21	22	WD#
GND	23	24	WE#
GND	25	26	TRAK0#
GND	27	28	WPT#
GND	29	30	RDATA#
GND	31	32	SIDE1#
GND	33	34	DSKCHG#

3.7.4 Signal Description – Floppy Connector (CN2)

RDATA#	The read data input signal from the FDD.
WD#	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	Write enable. An open drain output.
MOA#	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
MOB#	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DSA#	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DSB#	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	Direction of the head step motor. An open drain output Logic 1 = outward motion Logic 0 = inward motion
STEP#	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
DRV DEN0/1#	This output indicates whether a low drive density (250/300kbps at low level) or a high drive density (500/1000kbps at high level) has been selected.
TRAK0#	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
INDEX#	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
WP#	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
DSKCHG#	Diskette change. This signal is active low at power on and whenever the diskette is removed.

3.7.5 Parallel Port Connector (CN3)

Signal	PIN		Signal
GND	26	25	SLCT
GND	24	23	PE
GND	22	21	BUSY
GND	20	19	ACK#
GND	18	17	PD7
GND	16	15	PD6
GND	14	13	PD5
GND	12	11	PD4
GND	10	9	PD3
SLIN#	8	7	PD2
INIT#	6	5	PD1
ERR#	4	3	PD0
AFD#	2	1	STB#

3.7.6 Signal Description – Parallel Port Connector (CN3)

The following signal description covers the signal definitions, when the parallel port is operated in standard centronic mode. The parallel port controller also supports the fast EPP and ECP modes.

PD [7:0]	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Output line for detection of printer selection. This pin is pulled high internally.
SLCT	An active high input on this pin indicates that the printer is selected. This pin is pulled high internally.
STB#	An active low output is used to latch the parallel data into the printer. This pin is pulled high internally.
BUSY	An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally.
ACK#	An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally.
INIT#	Output line for the printer initialization. This pin is pulled high internally.
AFD#	An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally.
ERR#	An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally.
PE	An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.

3.7.7 Front Panel Connector (CN4)

Signal	PIN		Signal
SPKIN	14	7	GND
NC	13	6	PWRBT
NC	12	5	NC
+5V	11	4	HHLED
GND	10	3	+5V
NC	9	2	RESET
+5V	8	1	GND

3.7.8 Signal Description – Front Panel Connector (CN4)

HHLED	Power LED
PWRBT	Power Button
RESET	System Reset
SPKIN	External Speaker

3.7.9 Secondary IDE Connector (CN5)

Signal	PIN		Signal
RESET#	1	2	GND
DD7	3	4	DD8
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
GND	19	20	NC
DDRQ1	21	22	GND
DIOW1#	23	24	GND
DIOR1#	25	26	GND
DRDY1#	27	28	GND
DDACK1#	29	30	GND
IRQ15	31	32	NC
DA1	33	34	NC
DA0	35	36	DA2
DCS0#	37	38	DCS1#
DDACT1#	39	40	GND
+5V	41	42	+5V
GND	43	44	NC

3.7.10 Signal Description – Secondary IDE Connector (CN5)

DA [2:0]	IDE Address Bits These address bits are used to access a register or data port in a device on the IDE bus.
DCS [1:0]#	IDE Chip Selects The chip select signals are used to select the command block registers in an IDE device.
DD [15:0]	IDE Data Lines DD [15:0] transfers data to/from the IDE devices.
DIOR [1:0]#	IDE I/O Read for Channels 0 and 1 DIOR0# is the read signal for Channel 0, and DIOR1# is the read signal for Channel 1. Each signal is asserted on read accesses to the corresponding IDE port addresses.
DIOW [1:0]#	IDE I/O Write for Channels 0 and 1 DIOW0# is the write signal for Channel 0, and DIOW1# is the read signal for Channel 1. Each signal is asserted on write accesses to corresponding IDE port addresses.
DRDY [1:0]#	EIDE Mode: Primary / Secondary I/O Channel Ready. Device ready indicator. UltraDMA Mode: Primary / Secondary Device DMA Ready. Output flow control. The device may assert DDMARDY to pause output transfers. Primary Device Strobe. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers.
RESET#	IDE Reset This signal resets all the devices that are attached to the IDE interface.
IRQ14/15	Interrupt line from IDE device. Connected directly to PC-AT bus.
DDRQ [1:0]	DMA Request Channels 0 and 1 The DDRQ is used to request a DMA transfer from the CS5530A. The direction of the transfers are determined by the IDE_IOR/IOW signals.
DDACK [1:0]#	DMA Acknowledge Channels 0 and 1 The DACK# acknowledges the DREQ request to initiate DMA transfers.
DDACT [1:0]#	Signal from IDE device indicating IDE device activity. The signal level depends on the IDE device type, normally active low.

3.7.11 LCD panel Connector (CN6)

Signal	PIN		Signal
ENBKL	39	40	ENVEE
M	37	38	LP
SHFCLK	35	36	FLM
GND	33	34	GND
P22	31	32	P23
P20	29	30	P21
P18	27	28	P19
P16	25	26	P17
P14	23	24	P15
P12	21	22	P13
P10	19	20	P11
P8	17	18	P9
P6	15	16	P7
P4	13	14	P5
P2	11	12	P3
P0	9	10	P1
VCON	7	8	GND
+3.3V	5	6	+3.3V
GND	3	4	GND
+5V	1	2	+5V

3.7.12 Signal Description – LCD Panel Connector (CN6)

P [23:0]	Flat Panel Data bit 23 to bit 0
SHFCLK	Flat Panel Shift Clock. This is the pixel clock for Flat Panel Data
LP	DSTN LCD: Line Pulse TFT LCD: LCD Horizontal Sync
FLM	First Line Marker. Flat panel equivalent of VSYNC (vertical synchronization)
M	M-signal or Display Enable. This signal is used to indicate the active horizontal display time. FPR3E [7] is used to select 1 = M-signal 0 = Display Enable
ENBKL	Flat Panel Enable. This signal needs to become active after all panel voltages, clocks, and data are supplied. This signal also needs to become inactive before any panel voltages or control signals are removed. FPEN is part of the VESA FPD1-1B specification.
ENVEE	Flat Panel Voltage Bias Enable. This signal is used to control LCD Bias power.

3.7.13 Signal Configuration – DSTN & TFT Panel Displays (CN6)

Pin name	Color DSTN		Color TFT				
	16-bit	24-bit	9-bit	12-bit	18-bit	24-bit	12-bit x 2
P23		UD11				R7	RB3
P22		UD10				R6	RB2
P21		UD9			R5	R5	RB1
P20		UD8			R4	R4	RB0
P19	UD7	UD7		R3	R3	R3	RA3
P18	UD6	UD6	R2	R2	R2	R2	RA2
P17	UD5	UD5	R1	R1	R1	R1	RA1
P16	UD4	UD4	R0	R0	R0	R0	RA0
P15	UD3	UD3				G7	GB3
P14	UD2	UD2				G6	GB2
P13	UD1	UD1			G5	G5	GB1
P12	UD0	UD0			G4	G4	GB0
P11		LD11		G3	G3	G3	GA3
P10		LD10	G2	G2	G2	G2	GA2
P9		LD9	G1	G1	G1	G1	GA1
P8		LD8	G0	G0	G0	G0	GA0
P7	LD7	LD7				B7	BB3
P6	LD6	LD6				B6	BB2
P5	LD5	LD5			B5	B5	BB1
P4	LD4	LD4			B4	B4	BB0
P3	LD3	LD3		B3	B3	B3	BA3
P2	LD2	LD2	B2	B2	B2	B2	BA2
P1	LD1	LD1	B1	B1	B1	B1	BA1
P0	LD0	LD0	B0	B0	B0	B0	BA0

Note:

The principle of attachment of TFT panels is that the bits for red, green, and blue use the least significant bits and skip the most significant bits if the display interface width of the TFT panel is insufficient.

3.7.14 VGA Connector (CN7)

Signal	PIN		Signal
		6	GND
RED	1	11	NC
		7	GND
GREEN	2	12	DDCDAT
		8	GND
BLUE	3	13	HSYNC
		9	VCC
NC	4	14	VSYNC
		10	GND
GND	5	15	DDCCLK

3.7.15 Signal Description – VGA Connector (CN7)

HSYNC	CRT horizontal synchronisation output.
VSYNC	CRT vertical synchronisation output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 Ω cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 Ω cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 Ω cable impedance.

3.7.16 IrDA Connector (CN8)

Signal	PIN
IRTX	5
GND	4
IRRX	3
CIRRX	2
+5V	1

3.7.17 Signal Description – IrDA Connector (CN8)

IRRX	Infrared Receiver input
IRTX	Infrared Transmitter output

3.7.18 10/100 BASE-Tx Ethernet Connector (CN9)

Signal	PIN
NC	8
NC	7
RXD-	6
NC	5
NC	4
RXD+	3
TXD-	2
TXD+	1

3.7.19 Signal Description – 10/100Base-Tx Ethernet Connector (CN9)

TXD+ / TXD-	Ethernet 10/100Base-Tx differential transmitter outputs.
RXD+ / RXD-	Ethernet 10/100Base-Tx differential receiver inputs.

3.7.20 Serial Port 1 with External DB9 Connector (CN10)

Signal	PIN		Signal
GND	5		
		9	RI
DTR	4		
		8	CTS
TxD	3		
		7	RTS
RxD	2		
		6	DSR
DCD	1		

3.7.21 Serial port 2 Connector in RS-232 mode (CN11)

Signal	PIN		Signal
NC	10	9	RI
CTS	8	7	RTS
DSR	6	5	GND
DTR	4	3	TxD
RxD	2	1	DCD

3.7.22 Serial Port 2 Connector in RS-422 Mode (CN11)

Signal	PIN		Signal
NC	10	9	NC
NC	8	7	NC
NC	6	5	NC
Rx-	4	3	Tx+
Rx+	2	1	Tx-

3.7.23 Serial Port 2 Connector in RS-485 Mode (CN11)

Signal	PIN		Signal
NC	10	9	NC
NC	8	7	NC
NC	6	5	NC
NC	4	3	DATA+
NC	2	1	DATA-

3.7.24 Signal Description – Serial Port 1 / 2 Connector in RS-232 Mode (CN10/11)

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

3.7.25 Signal Description – Serial Port 2 in RS-422 Mode (CN11)

Tx +/-	Serial output. This differential signal pair sends serial data to the communication link. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication link, if the RTS register of the Serial Port 2 is set to LOW.
Rx +/-	Serial input. This differential signal pair receives serial data from the communication link. Received data is available in Serial Port 2 Receiver Buffer Register.

3.7.26 Signal Description – Serial Port 2 in RS-485 Mode (CN11)

DATA +/-	This differential signal pair sends and receives serial data to the communication link. The mode of this differential signal pair is controlled through the RTS register of Serial Port 2. Set the RTS register of the Serial Port 2 to LOW for transmitting, HIGH for receiving.
----------	---

Warning: Do not select a mode different from the one used by the connected peripheral, as this may damage CPU board and/or peripheral.

The transmitter drivers in the port are short circuit protected by a thermal protection circuit. The circuit disables the drivers when the die temperature reach 150 °C.

RS-422 mode is typically used in point to point communication. Data and control signal pairs should be terminated in the receiver end with a resistor matching the cable impedance (typ. 100-120 Ω). The resistors could be placed in the connector housing.

RS-485 mode is typically used in multi drop applications, where more than 2 units are communicating. The data and control signal pairs should be terminated in each end of the communication line with a resistor matching the cable impedance (typical 100-120 Ω). Stubs to substations should be avoided.

3.7.27 Auxiliary Power Connector (CN12)

Signal	PIN
-12V	4
GND	3
GND	2
-5V	1

3.7.28 Internal Keyboard Connector (CN13)

Signal	PIN
+5V	5
GND	4
NC	3
KBDT	2
KBCK	1

3.7.29 Keyboard and PS/2 Mouse Connector (CN14)

Signal	PIN		Signal
MCLK	6	5	KCLK
VCC	4	3	GND
MDAT	2	1	KDAT

3.7.30 Signal Description – Keyboard & PS/2 Mouse Connectors (CN14)

KCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.
MCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.

3.7.31 TV Output Connector (CN15)

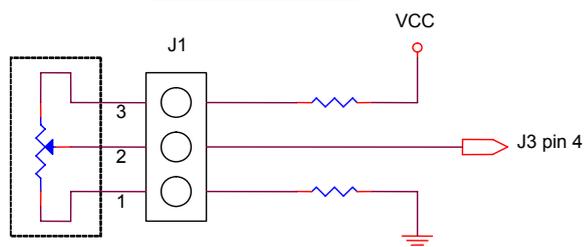
Signal	PIN
CVBS	1
GND	2
Y	3
C	4
GND	5

3.7.32 Signal Description – TV Output Connector (CN15)

Y	Luminance output
C	Chrominance
CVBS	Composit Video output

3.7.33 LCD Backlight Brightness Adjustment Connector (J1)

Signal	PIN
+5V	3
VR	2
GND	1



Variation Resistor (Recommended: 4.7KΩ, >1/16W)

3.7.34 LCD Backlight Contrast Adjustment Connector (J2)

Signal	PIN
+3.3V	3
Vcon	2
GND	1

3.7.35 LCD Inverter Connector (J3)

Signal	PIN
+12V	1
GND	2
ENBKL	3
VR	4
+5V	5

Note:

For inverters with adjustable Backlight function, it is possible to control the LCD brightness through the VR signal controlled by **J1**. Please see the **J1** section for detailed circuitry information.

3.7.36 Power Connector (J4)

PIN	Signal
1	PSON#
2	+5V
3	VCCSB

Note:

Set J4 to 2-3 closed if AT power supply is to be used.

3.7.37 Digital I/O Connector (J10)

Signal	PIN		Signal
DO3	7	8	DI3
DO2	5	6	DI2
DO1	3	4	DI1
DO0	1	2	DI0

3.7.38 Digital Input / Output Programming (J10)

The ECB-641 series uses digital I/O to customize its configuration to your control needs. For example, you may configure the digital I/O to control the opening and closing of the cash drawer or to sense the warning signal from a tripped UPS. The following is a detailed description of how the digital I/O is controlled via software programming:

Digital Inputs	Address	Bit
DI1	281	1
DI2	281	2
DI3	281	3
DI4	281	4
Digital Outputs	Address	Bit
DO1	280	1
DO2	280	2
DO3	280	3
DO4	280	4

3.7.39 PC/104 Connector (P1, P2)

Signal	PIN		PIN		Signal
GND	B32	A32			GND
GND	B31	A31			SA0
OSC	B30	A30			SA1
VCC	B29	A29			SA2
BALE	B28	A28			SA3
NC			C19	D19	GND
TC	B27	A27			SA4
SD15			C18	D18	GND
DACK2#	B26	A26			SA5
SD14			C17	D17	MASTER#
IRQ3	B25	A25			SA6
SD13			C16	D16	VCC
IRQ4	B24	A24			SA7
SD12			C15	D15	DRQ7
IRQ5	B23	A23			SA8
SD11			C14	D14	DACK7#
IRQ6	B22	A22			SA9
SD10			C13	D13	DRQ6
IRQ7	B21	A21			SA10
SD9			C12	D12	DACK6#
SYSCLK	B20	A20			SA11
SD8			C11	D11	DRQ5
REFRESH#	B19	A19			SA12
SMEMW#			C10	D10	DACK5#
DRQ1	B18	A18			SA13
SMEMR#			C9	D9	DRQ0
DACK1#	B17	A17			SA14
LA17			C8	D8	DACK0#
DRQ3	B16	A16			SA15
LA18			C7	D7	IRQ14
DACK3#	B15	A15			SA16
LA19			C6	D6	IRQ15
IOR#	B14	A14			SA17
LA20			C5	D5	IRQ12
IOW#	B13	A13			SA18
LA21			C4	D4	IRQ11
SMEMR#	B12	A12			SA19
LA22			C3	D3	IRQ10
SMEMW#	B11	A11			AEN
LA23			C2	D2	IOCS16#
GND	B10	A10			IOCHRDY
SBHE#			C1	D1	MEMCS16#
+ 12 V	B9	A9			SD0
GND			C0	D0	GND
OVS#	B8	A8			SD1
- 12 V	B7	A7			SD2
DRQ2	B6	A6			SD3
- 5 V	B5	A5			SD4
IRQ9	B4	A4			SD5
VCC	B3	A3			SD6
RESETDRV	B2	A2			SD7
GND	B1	A1			IOCHCHK#

3.7.40 Signal Description – PC/104 Connector (P1, P2)

3.7.40.1 Address

LA [23:17]	The address signals LA [23:17] define the selection of a 128KB section of memory space within the 16MB address range of the 16-bit data bus. These signals are active high. The validity of the MEMCS16# depends on these signals only. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case, the temporary master drives these lines. The LA signals are not defined for I/O accesses.
SA [19:0]	System address. Address lines for the first one Megabyte of memory. SA [9:0] used for I/O addresses. SA0 is the least significant bit
SBHE#	This signal is an active low signal, that indicates that a byte is being transferred on the upper byte (SD [15:8]) of the 16 bit bus. All bus masters will drive this line with a tri-state driver.

3.7.40.2 Data

SD [15:8]	These signals are defined for the high order byte of the 16-bit data bus. Memory or I/O transfers on this part of the bus are defined when SBHE# is active.																									
SD [7:0]	These signals are defined for the low order byte of the 16-bit data bus being the only bus for 8 bit PC-AT/PC104 adapter boards. Memory or I/O transfers on this part of the data bus are defined for 8-bit operations with even or odd addresses and for 16-bit operations for odd addresses only. The signals SA0 and SBHE# are used to define the data present on this bus: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SBHE#</th> <th>SA0</th> <th>SD15-SD8</th> <th>SD7-SD0</th> <th>Action</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>ODD</td> <td>EVEN</td> <td>Word transfer</td> </tr> <tr> <td>0</td> <td>1</td> <td>ODD</td> <td>ODD</td> <td>Byte transfer on SD15-SD8</td> </tr> <tr> <td>1</td> <td>0</td> <td>-</td> <td>EVEN</td> <td>Byte transfer on SD7-SD0</td> </tr> <tr> <td>1</td> <td>1</td> <td>-</td> <td>ODD</td> <td>Byte transfer on SD7-</td> </tr> </tbody> </table>	SBHE#	SA0	SD15-SD8	SD7-SD0	Action	0	0	ODD	EVEN	Word transfer	0	1	ODD	ODD	Byte transfer on SD15-SD8	1	0	-	EVEN	Byte transfer on SD7-SD0	1	1	-	ODD	Byte transfer on SD7-
SBHE#	SA0	SD15-SD8	SD7-SD0	Action																						
0	0	ODD	EVEN	Word transfer																						
0	1	ODD	ODD	Byte transfer on SD15-SD8																						
1	0	-	EVEN	Byte transfer on SD7-SD0																						
1	1	-	ODD	Byte transfer on SD7-																						

3.7.40.3 Commands

BALE	This is an active high signal used to latch valid addresses from the current bus master on the falling edge of BALE. During DMA, refresh and alternate master cycles, BALE is forced high for the duration of the transfer. BALE is driven by the permanent master with a totem-pole driver.
IOR#	This is an active low signal driven by the current master to indicate an I/O read operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with DACK _n # to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
IOW#	This is an active low signal driven by the current master to indicate an I/O write operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with DACK _n # to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
SMEMR#	This is an active low signal driven by the permanent master to indicate a memory read operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
SMEMW#	This is an active low signal driven by the permanent master to indicate a memory write operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMR#	This is an active low signal driven by the current master to indicate a memory read operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMW#	This is an active low signal driven by the current master to indicate a memory write operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.

3.7.40.4 Transfer Response

IOCS16#	This is an active low signal driven by an I/O-mapped PC-AT/PC104 adapter indicating that the I/O device located at the address is a 16-bit device. This open collector signal is driven, based on SA [15:0] only (not IOR# and IOW#) when AEN is not asserted.
MEMCS16#	This is an active low signal driven by a memory mapped PC-AT/PC104 adapter indicating that the memory device located at the address is a 16-bit device. This open collector signal is driven, based on LA [23:17] only.
OWS#	This signal is an active low open-collector signal asserted by a 16-bit memory mapped device that may cause an early termination of the current transfer. It should be gated with MEMR# or MEMW# and is not valid during DMA transfers. IOCHRDY precedes OWS#.
IOCHRDY	This is an active high signal driven inactive by the target of either a memory or an I/O operation to extend the current cycle. This open collector signal is driven based on the system address and the appropriate control strobe. IOCHRDY precedes OWS#.
IOCHCK#	This is an active low signal driven active by a PC-AT/PC104 adapter detecting a fatal error during bus operation. When this open collector signal is driven low it will typically cause a non-maskable interrupt.

3.7.40.5 Controls

SYCLK	This clock signal may vary in frequency from 2.5 MHz to 25.0 MHz depending on the setup made in the BIOS. Frequencies above 16 MHz are not recommended. The standard states 6 MHz to 8.33 MHz, but most new adapters are able to handle higher frequencies. The PC-AT/PC104 bus timing is based on this clock signal.
OSC	This is a clock signal with a 14.31818 MHz \pm 50 ppm frequency and a 50 \pm 5% duty cycle. The signal is driven by the permanent master.
RESETDRV	This active high signal indicates that the adapter should be brought to an initial reset condition. This signal will be asserted by the permanent master on the bus for at least 100 ns at power-up or watchdog time-out to ensure that adapters in the system are properly reset. When active, all adapters should turn off or tri-state all drivers connected to the bus.

3.7.40.6 Interrupts

IRQ [3:7], IRQ [9:12], IRQ [14:15]	These signals are active high signals, which indicate the presence of an interrupting PC-AT/PC104 bus adapter. Due to the use of pull-ups, unused interrupt inputs must be masked.
--	--

3.7.40.7 Bus Arbitration

DRQ [0:3], DRQ [5:7]	These signals are active high signals driven by a DMA bus adapter to indicate a request for a DMA bus operation. DRQ [0:3] request 8 bit DMA operations, while DRQ [5:7] request 16 bit operations. All bus DMA adapters will drive these lines with a tri-state driver. The permanent master monitors these signals to determine which of the DMA devices, if any, are requesting the bus.
DACK [0:3]#, DACK [5:7]#	These signals are active low signals driven by the permanent master to indicate that a DMA operation can begin. They are continuously driven by a totem pole driver for DMA channels attached.
AEN	This signal is an active high totem pole signal driven by the permanent master to indicate that the address lines are driven by the DMA controller. The assertion of AEN disables response to I/O port addresses when I/O command strobes are asserted. AEN being asserted, only the device with active DACK _n # should respond.
REFRESH#	This is an active low signal driven by the current master to indicate a memory refresh operation. The current master will drive this line with a tri-state driver.
TC	This active high signal is asserted during a read or write command indicating that the DMA controller has reached a terminal count for the current transfer. DACK _n # must be presented by the bus adapter to validate the TC signal.
MASTER#	This signal is not supported by the chipset.

4. AWARD BIOS Setup

4.1 Starting Setup

The AwardBIOS™ is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing immediately after switching the system on, or

By pressing the key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

Press F1 To Continue, DEL to enter SETUP

4.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item in the left hand
Right arrow	Move to the item in the right hand
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

Table 1: Legend Keys

4.2.1 Navigating Through The Menu Bar

Use the left and right arrow keys to choose the menu you want to be in.

4.2.2 To Display a Sub Menu

Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A "➤" pointer marks all sub menus.

4.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

4.4 In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the Award BIOS™ supports an override to the CMOS settings which resets your system to its defaults.

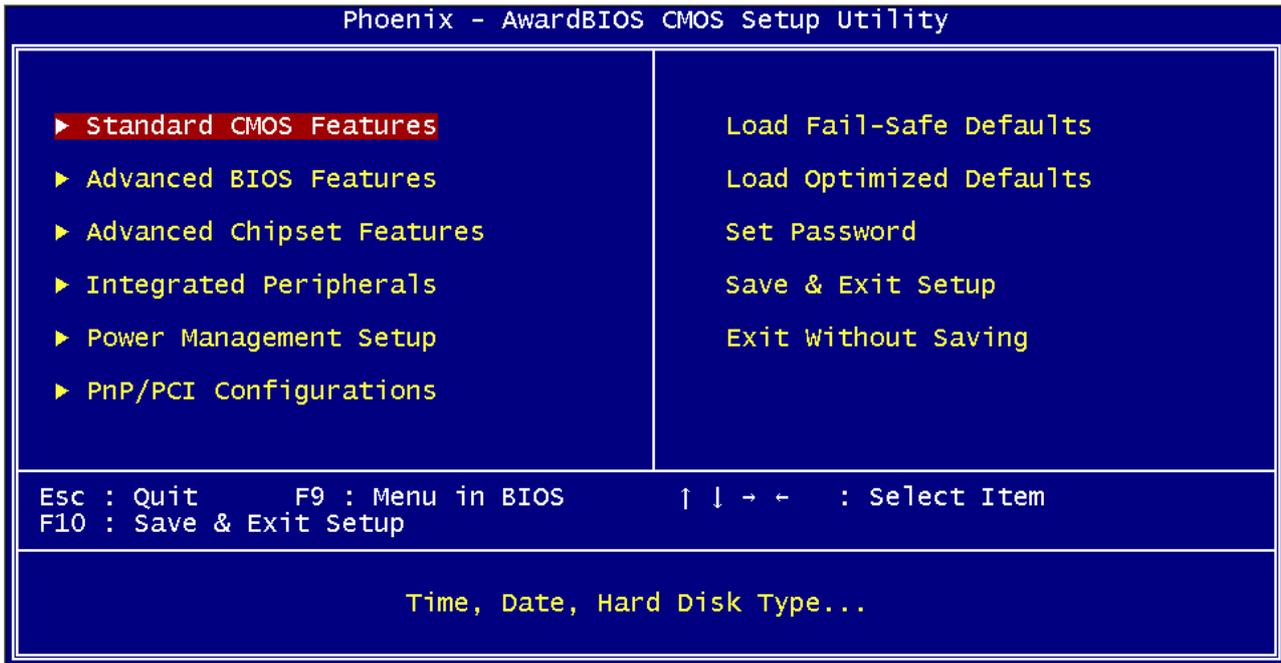
The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

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4.5 Main Menu

Once you enter the Award BIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

Note that a brief description of each highlighted selection appears at the bottom of the screen.



4.5.1 Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

4.5.1.1 Standard CMOS Features

Use this menu for basic system configuration.

4.5.1.2 Advanced BIOS Features

Use this menu to set the Advanced Features available on your system.

4.5.1.3 Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system's performance.

4.5.1.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

4.5.1.5 Power Management Setup

Use this menu to specify your settings for power management.

4.5.1.6 PNP / PCI Configuration

This entry appears if your system supports PnP / PCI.

4.5.1.7 Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

4.5.1.8 Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

4.5.1.9 Set Password

Use this menu to set Passwords.

4.5.1.10 Save & Exit Setup

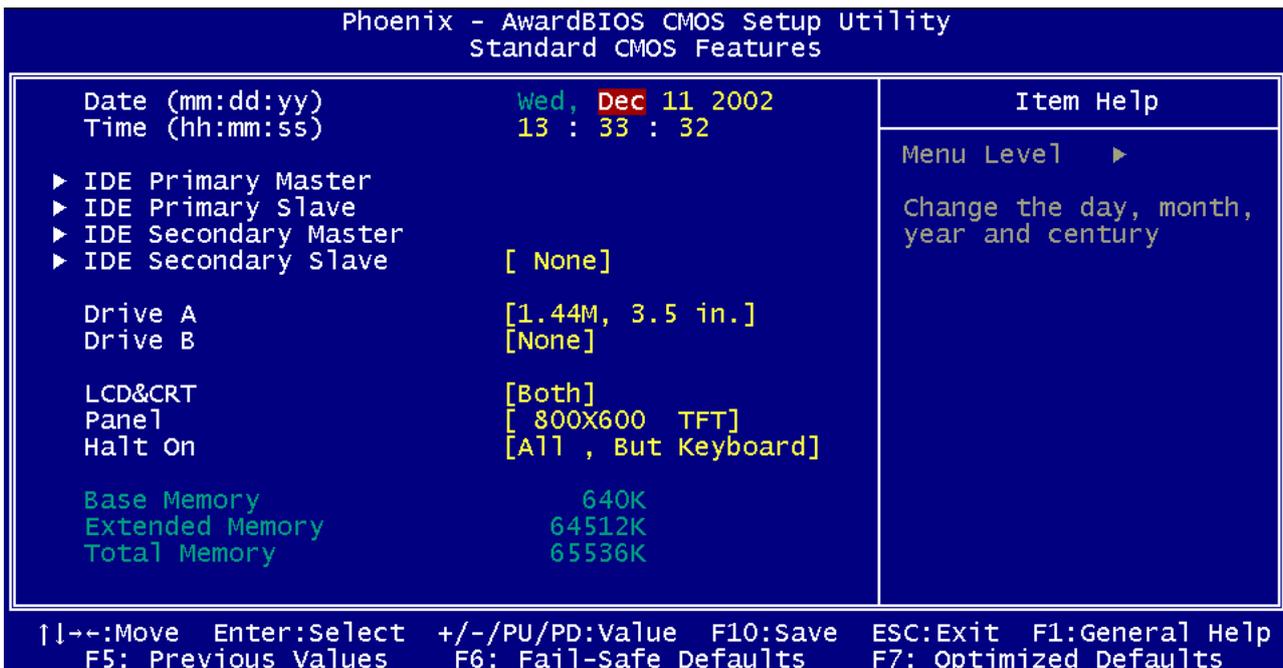
Save CMOS value changes to CMOS and exit setup.

4.5.1.11 Exit Without Save

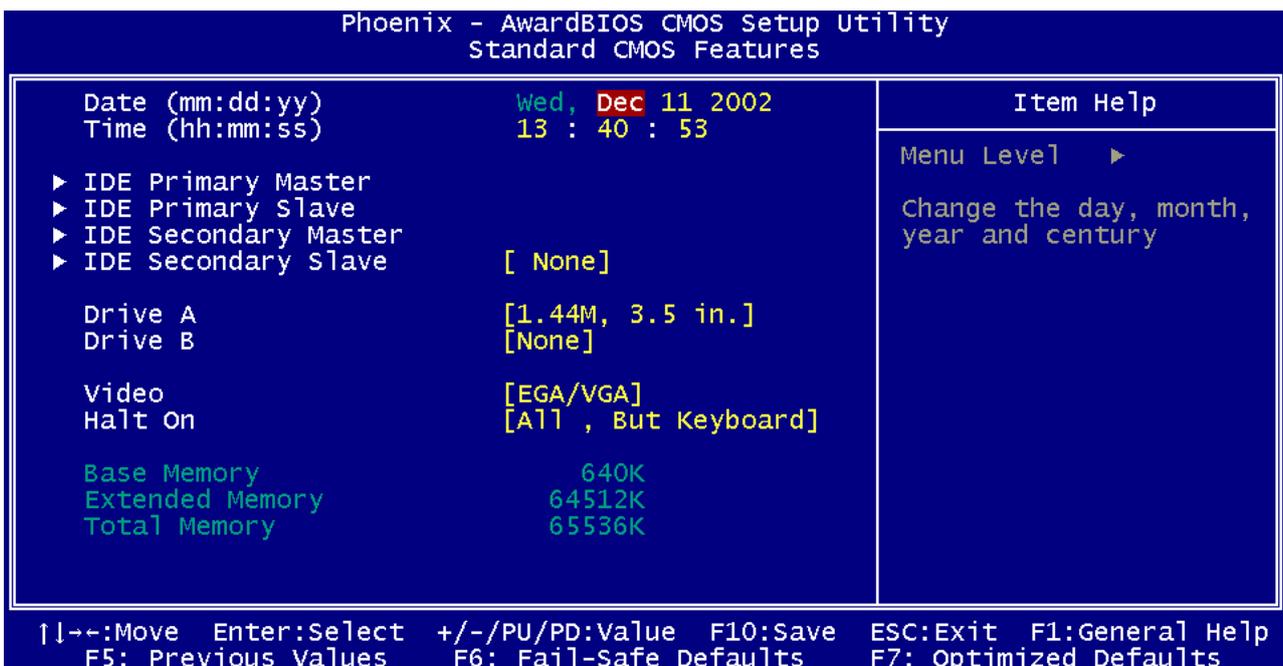
Abandon all CMOS value changes and exit setup.

4.5.2 Standard CMOS Setup

The items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.



ECB-641



ECB-641C

4.5.2.1 Standard CMOS setup menu

This table shows the selections that you can make on the Main Menu.

Item	Options	Description
Date	Month DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
IDE Primary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Primary Slave	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
Drive A Drive B	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
LCD&CRT	BOTH LCD CRT	Select the type of video adapter (SMI 712/721) device
Panel	640x480 TFT 640x480 DSTN 800x600 TFT 800x600 DSTN 1024x768 TFT 1024x768 DSTN 1280x1024 TFT	Select the type of LCD panel
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you
Base Memory	N/A	Displays the amount of conventional memory detected during boot up
Extended Memory	N/A	Displays the amount of extended memory detected during boot up
Total Memory	N/A	Displays the total memory available in the system

Table 2: Main Menu Selections (ECB-641)

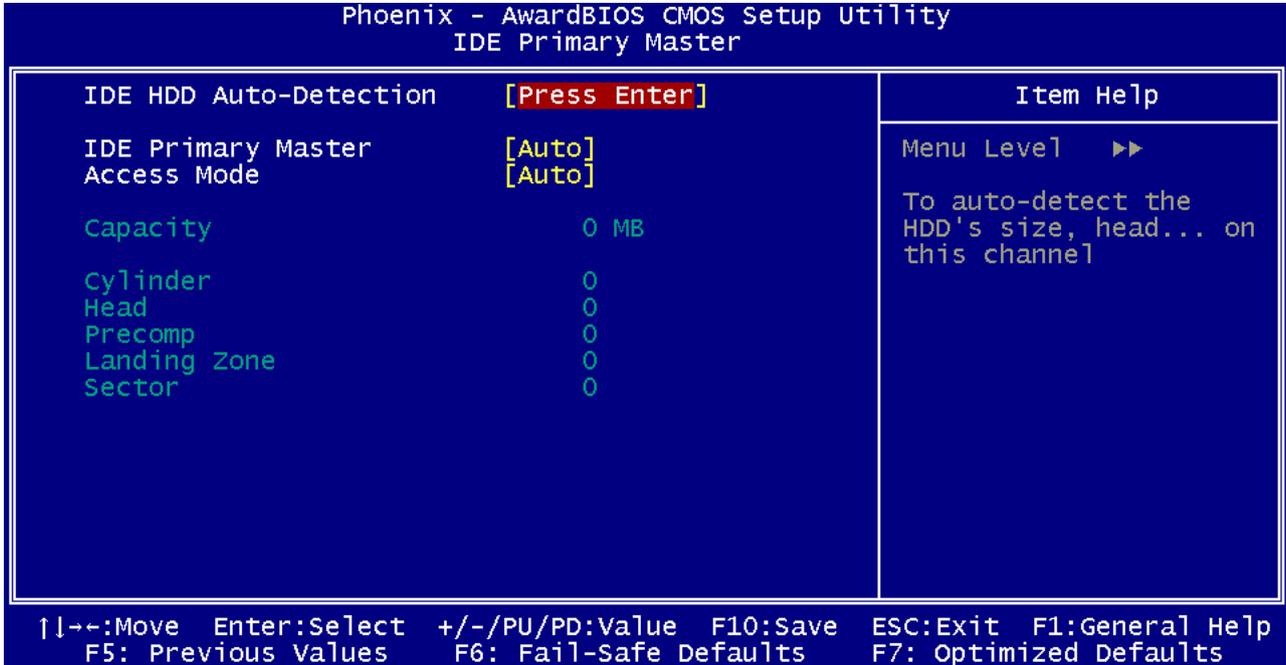
Item	Options	Description
Date	Month DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
IDE Primary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Primary Slave	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
Drive A Drive B	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you
Base Memory	N/A	Displays the amount of conventional memory detected during boot up
Extended Memory	N/A	Displays the amount of extended memory detected during boot up
Total Memory	N/A	Displays the total memory available in the system

Table 2: Main Menu Selections (ECB-641C)

4.5.2.2 IDE Adapters

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive.

Figure 2 shows the IDE primary master sub menu.



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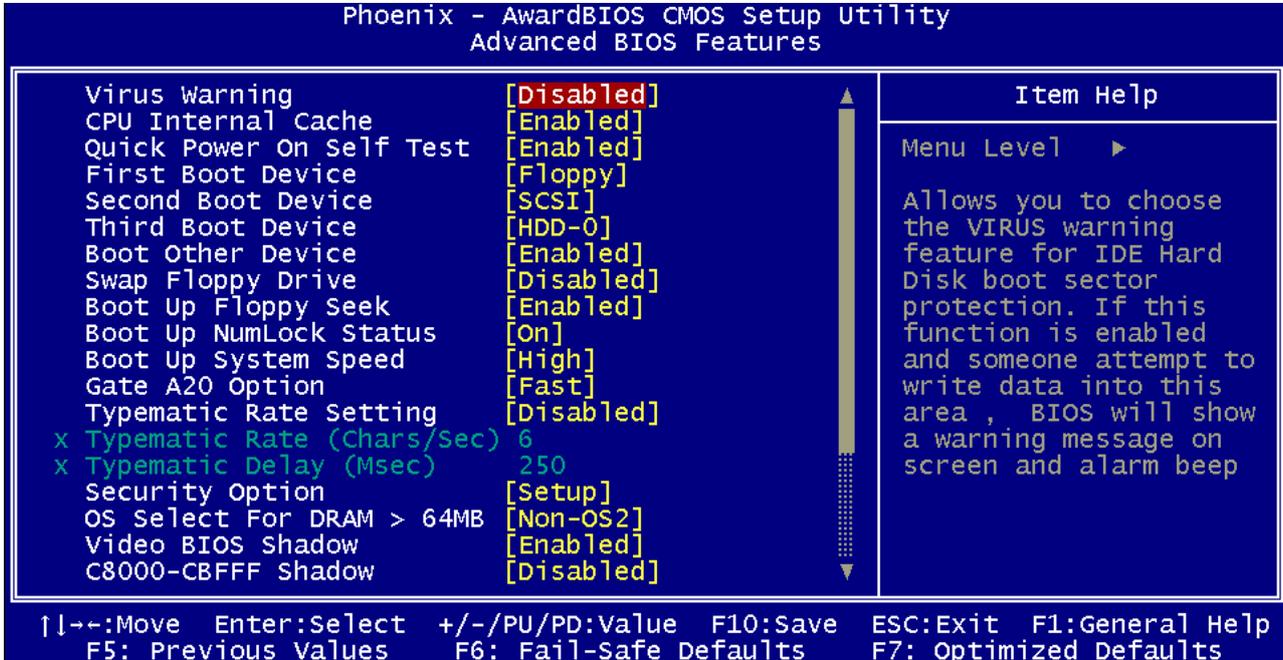
Use the legend keys to navigate through this menu and exit to the main menu. Use Table 3 to configure the hard disk.

Item	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Capacity	Auto Display your disk drive size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
Access Mode	Normal LBA Large Auto	Choose the access mode for this hard disk
The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'		
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** Warning: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

Table 3: Hard disk selections

4.5.3 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



4.5.3.1 Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

4.5.3.2 CPU Internal Cache

This item allows you to speed up memory access. However, it depends on CPU design.

Enabled	Enable cache
Disabled	Disable cache

4.5.3.3 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enable quick POST
Disabled	Normal POST

4.5.3.4 First/Second/Third/Other Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

Floppy	Floppy Device
HDD-0	First Hard Disk Device
SCSI	SCSI Device
CDROM	CDROM Device
HDD-1	Secondary Hard Disk Device
HDD-2	Third Hard Disk Device
HDD-3	Fourth Hard Disk Device
LAN	Lan Device
Disabled	Disabled any boot device

4.5.3.5 Boot Up Floppy Seek

Seeks disk drives during boot up. Disabling speeds boot up.

Enabled	Enable Floppy Seek
Disabled	Disable Floppy Seek

4.5.3.6 Swap Floppy Drive

Swap floppy disk drives A & B during boot up.

Enabled	Enable Floppy swap A & B
Disabled	Disable Floppy swap A & B

4.5.3.7 Boot Up NumLock Status

Select power on state for NumLock.

Enabled	Enable NumLock
Disabled	Disable NumLock

4.5.3.8 Gate A20 Option

Select if chipset or keyboard controller should control GateA20.

Normal	A pin in the keyboard controller controls GateA20
Fast	Lets chipset control GateA20

4.5.3.9 Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

The choice: Enabled/Disabled.

4.5.3.10 Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a key stroke when you hold the key down.

The choice: 6, 8, 10, 12, 15, 20, 24, or 30.

4.5.3.11 Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke.

The choice: 250, 500, 750, or 1000.

4.5.3.12 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note:

To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

4.5.3.13 OS Select for DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.

The choice: Non-OS2, OS2

4.5.3.14 Video BIOS Shadow

Determines whether video BIOS will be copied to RAM. However, it is optional depending on chipset design. Video Shadow will increase the video speed.

Enabled	Video shadow is enabled
Disabled	Video shadow is disabled

4.5.3.15 C8000 – CBFFF Shadow/DC000 – DFFFF Shadow

These categories determine whether option ROMs will be copied to RAM. An example of such option ROM would be support of on-board SCSI.

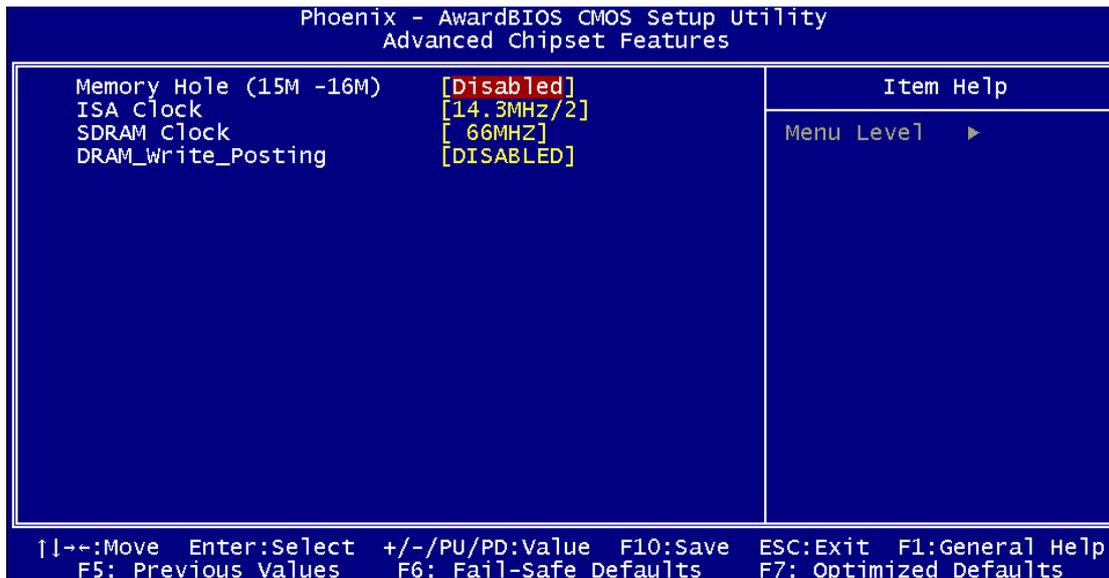
Enabled	Optional shadow is enabled
Disabled	Optional shadow is disabled

4.5.3.16 Small Logo (EPA) Show

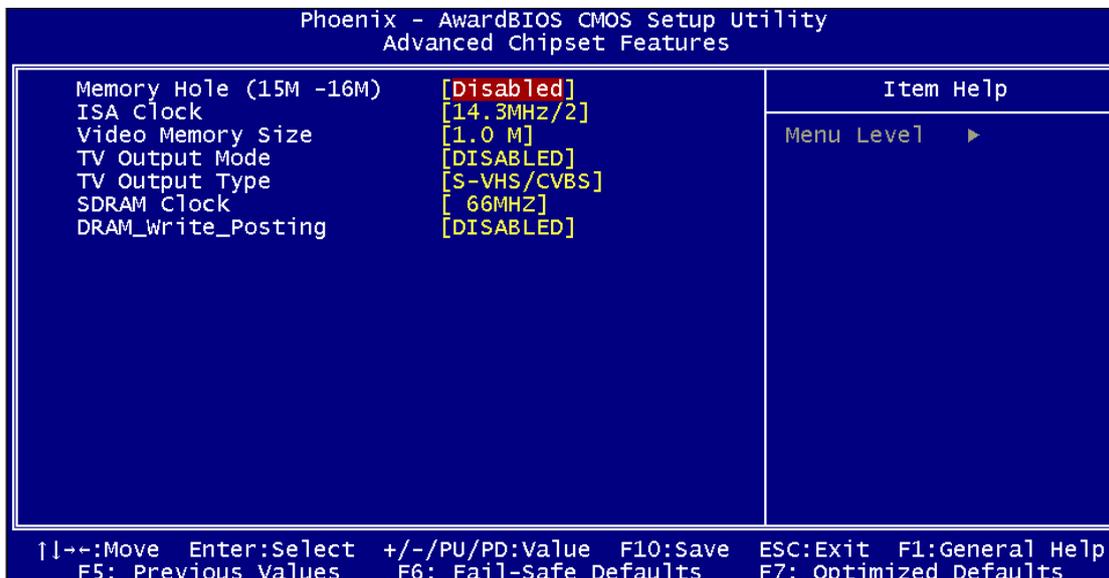
This item allows you enabled/disabled the small EPA logo show on screen at the POST step,

Enabled	EPA Logo show is enabled
Disabled	EPA Logo show is disabled

4.5.4 Advanced Chipset Features



ECB-641



ECB-641C

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.

4.5.4.1 Memory Hole (15M– 16M)

In order to improve performance, certain space in memory is reserved for ISA cards. This memory must be mapped into the memory space below 16MB.

The Choice: 15M-16M, Disabled.

4.5.4.2 ISA Clock

This item allows you to set ISA interface clock signal timing.

The Choice: 14.3MHz/2, PCICLK/4

4.5.4.3 Video Memory Size (ECB-641C)

This item allows you to select the video memory size, it's share system memory.

The Choice: None, 512K, 1.0M, 2.0M, 4.0M

4.5.4.4 TV Output Mode (ECB-641C)

This item allows you to select the TV output is enabled or disabled.

The Choice: Enabled, Disabled

4.5.4.5 TV Output Type (ECB-641C)

This item allows you to select the TV output type.

The Choice: S-VHS/CVBS, RGB

4.5.4.6 SDRAM Clock

This item allows you to set DRAM clock speed.

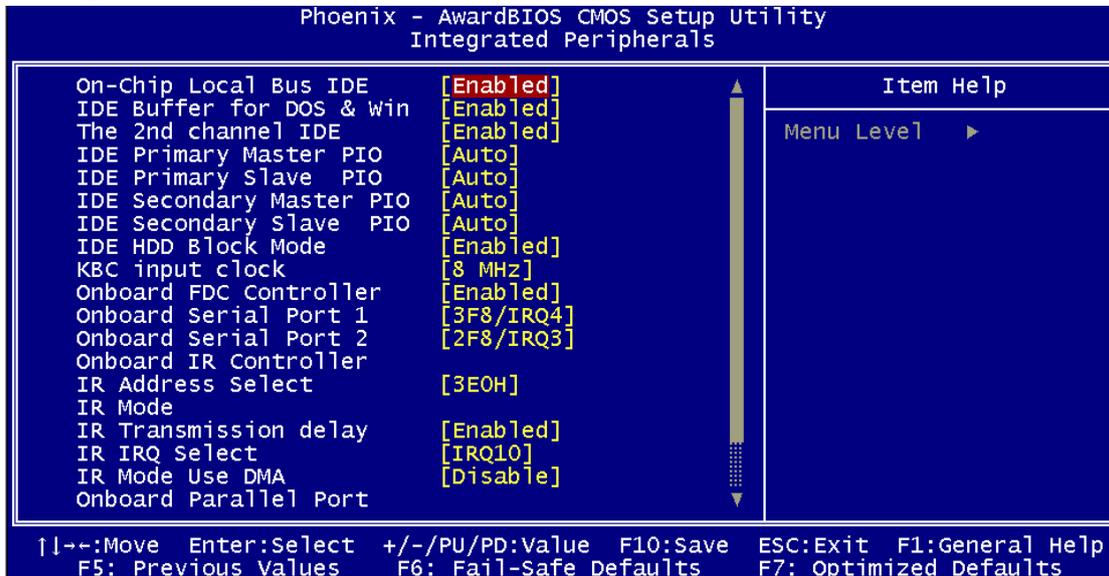
The Choice: 40MHz, 50MHz, 55MHz, 60MHz, 66MHz, 75MHz, 80MHz, 85MHz, 90MHz, 95MHz, 100MHz, 105MHz, 110MHz, 115MHz, 120MHz.

4.5.4.7 DRAM_Write_Posting

This item allows you to enabled or disabled DRAM write posting.

The Choice: Enabled, Disabled.

4.5.5 Integrated Peripherals



4.5.5.1 On-Chip Local Bus IDE

The chipset contains a local IDE interface with support for two IDE channels. Select Enabled to activate the primary IDE interface. Select Disabled to deactivate this interface.

The choice: Enabled, Disabled.

4.5.5.2 IDE Buffer for DOS & Win

The item allows you to disabled or enabled the IDE interface data transfer buffer for DOS and Windows OS environment.

The choice: Enabled, Disabled.

4.5.5.3 The choice: Enabled, Disabled The 2nd Channel IDE

The chipset contains a IDE interface with support for two IDE channels. Select Enabled to activate the secondary IDE interface. Select Disabled to deactivate this interface.

The choice: Enabled, Disabled.

4.5.5.4 Primary/Secondary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.

The choice: Auto, Mode 0, Mode 1, Mode 2, Mode 3, or Mode 4.

4.5.5.5 IDE HDD Block Mode

Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.

The Choice: Enabled, Disabled.

4.5.5.6 KBC Input clock

Select the Keyboard interface clock timing.

The Choice: 6 MHz, 8 MHz, 12 MHz, 16 MHz

4.5.5.7 Onboard FDC Controller

Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install and-in FDC or the system has no floppy drive, select Disabled in this field.

The Choice: Enabled, Disabled.

4.5.5.8 Onboard Serial Port 1/Port2

Select an address and corresponding interrupt for the first and second serial ports.

The choice: 3F8/IRQ4, 2E8/IRQ3, 3E8/IRQ4, 2F8/IRQ3, Disabled, Auto.

4.5.5.9 Onboard IR Controller

Select onboard IR Port (UART 3) controller operation mode.

The choice: Enabled, Disabled.

4.5.5.10 IR Address Select

Select the IR Port decode address

The Choice: 3F8H, 3E8H, 2F8H, 2E8H, 3E0H, 2E0H.

4.5.5.11 IR Mode

Select the IR Port operation mode

The Choice: IrDA, ASKIR, FIR

4.5.5.12 IR IRQ Select

Select the IR Port IRQ level.

The Choice: IRQ3, IRQ4, IRQ10, IRQ11.

4.5.5.13 Onboard Parallel Port

Select a logical LPT port name and matching address for the physical parallel (printer) port.

The choice: 378H/IRQ7, 278H/IRQ5, 3BCH/IRQ7, Floppy, Disabled.

4.5.5.14 Onboard Parallel Mode

Select an operating mode for the onboard parallel port. Select Compatible or Extended unless you are certain both your hardware and software support EPP or ECP mode.

The choice: EPP, ECP, ECP/EPP, Normal,

4.5.5.15 ECP Mode Use DMA

Select a DMA channel for the port.

The choice: 3, 1.

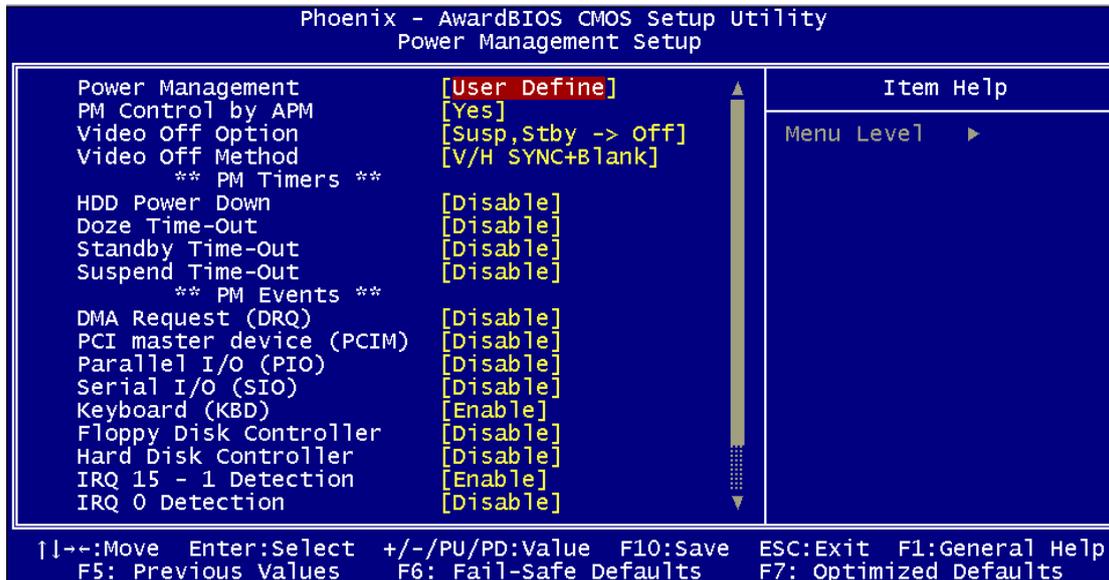
4.5.5.16 Parallel Port EPP Type

Select EPP port type 1.7 or 1.9.

The choice: EPP1.7, EPP1.9.

4.5.6 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.



4.5.6.1 Power Management

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

1. Standby Mode
2. HDD Power Down

There are two selections for Power Management; both of them have fixed mode settings.

Disable (default)	No power management. Disables all four modes
Min. Power Saving	Standby Time-Out = 2 min, Suspend Time-out = 4 min.
Max. Power Saving	Standby Time-Out = 16 min, Suspend Time-Out=64 min.
User Defined	Allows you to set each mode individually. When not disabled, the ranges are list as follow: HDD Power Down : 2 Min to 15 Min and disable Doze Time-Out : 50ms to 16 second and disable Standard Time-Out: 2 min. to 16 min Suspend Time-Out: 4 min. to 64 min. and disable.

4.5.6.2 PM Control by APM

This item allows you to enable/disable the Advanced Power Management (APM) function.

The choice: Enable, Disable.

4.5.6.3 Video Off Method

This determines the manner in which the monitor is blanked.

V/H SYNC+Blank	This selection will cause the system to turn off the vertical and horizontal synchronization ports and write blanks to the video buffer.
Blank Screen	This option only writes blanks to the video buffer.
DPMS	Initial display power management signaling.

4.5.6.4 PM Events

PM events are I/O events whose occurrence can prevent the system from entering a power saving mode or can awaken the system from such a mode. In effect, the system remains alert for anything which occurs to a device which is configured as *On*, even when the system is in a power down mode.

4.5.6.4.1 DMA Request (DRQ) / PCI Master Device (PCIM)

When you are *On of DMA / ISA Master or PCI Master*, any activity from one of the list system peripheral devices wakes up the system.

4.5.6.4.2 Parallel I/O (PIO) / Serial I/O(SIO) / Keyboard (KBD)

When *select PIO/SIO enable*, any activity from one of the listed system peripheral devices or IRQs wakes up the system.

4.5.6.4.3 Floppy Disk Controller/ Hard Disk Controller

When *select enable*, any activity from one of the listed system peripheral devices wakes up the system.

4.5.6.5 LAN & RING WAKE UP

This item allows you to determine that an input signal on the serial Ring Indicator (RI) line (in other words, an incoming call on the modem) power on the system from a soft off state.

The Choice: Enable, Disable

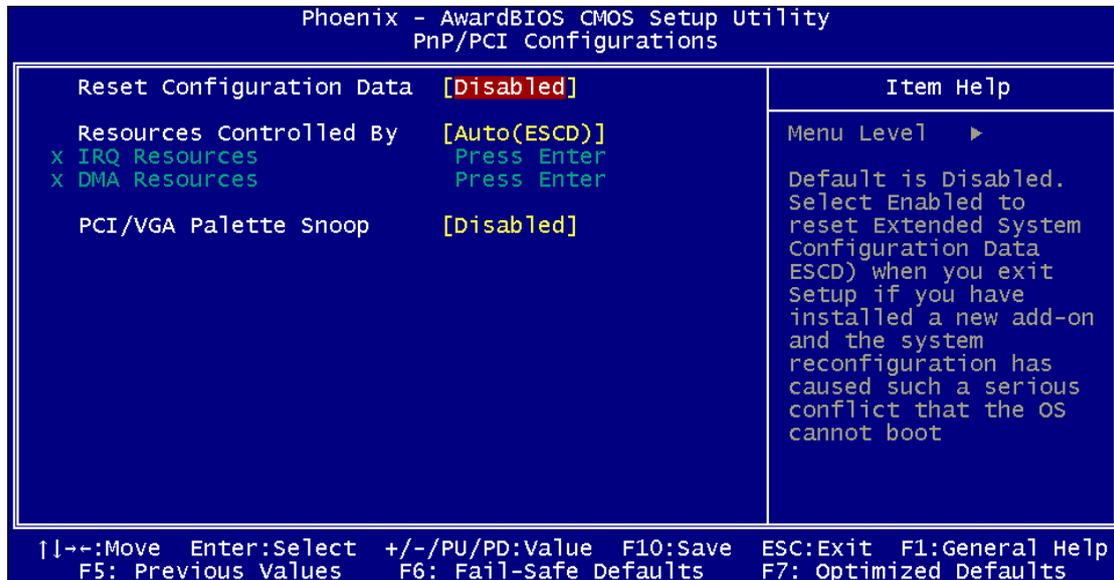
4.5.6.6 Soft-Off by POWER-Button

Pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has "hung".(Only could working on ATX Power supply)

The choice: Delay 4 Sec, Instant-Off

4.5.7 PnP/PCI Configuration Setup

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.



4.5.7.1 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

The choice: Enabled, Disabled.

4.5.7.2 Resource Controlled by

The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. If you set this field to “manual” choose specific resources by going into each of the sub menu that follows this field (a sub menu is preceded by a “▶”).

The choice: Auto, Manual.

4.5.7.3 IRQ Resources

When resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.

4.5.7.4 IRQ3/4/5/7/9/10/11/12/14/15 Assigned to

This item allows you to determine the IRQ assigned to the ISA bus and is not available to any PCI slot. Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.

The Choice: *Legacy ISA* and *PCI/ISA PnP*.

4.5.7.5 DMA Resources

When resources are controlled manually, assign each system DMA channel a type, depending on the type of device using the DMA channel.

4.5.7.6 DMA 0/1/3/5/6/7 Assigned to

Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.

Choices are *Legacy ISA* and *PCI/ISA PnP*.

4.5.7.7 PCI / VGA Palette Snoop

Leave this field at *Disabled*.

Choices are Enabled, Disabled.

4.5.8 Load Fail-Safe Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:



Pressing 'Y' loads the BIOS default values for the most stable, minimal-performance system operations.

4.5.9 Load Optimized Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:



Pressing 'Y' loads the default values that are factory settings for optimal performance system operations.

4.5.10 Set Password



The password setup function is for enter and change the options of the setup menus. When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD:

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

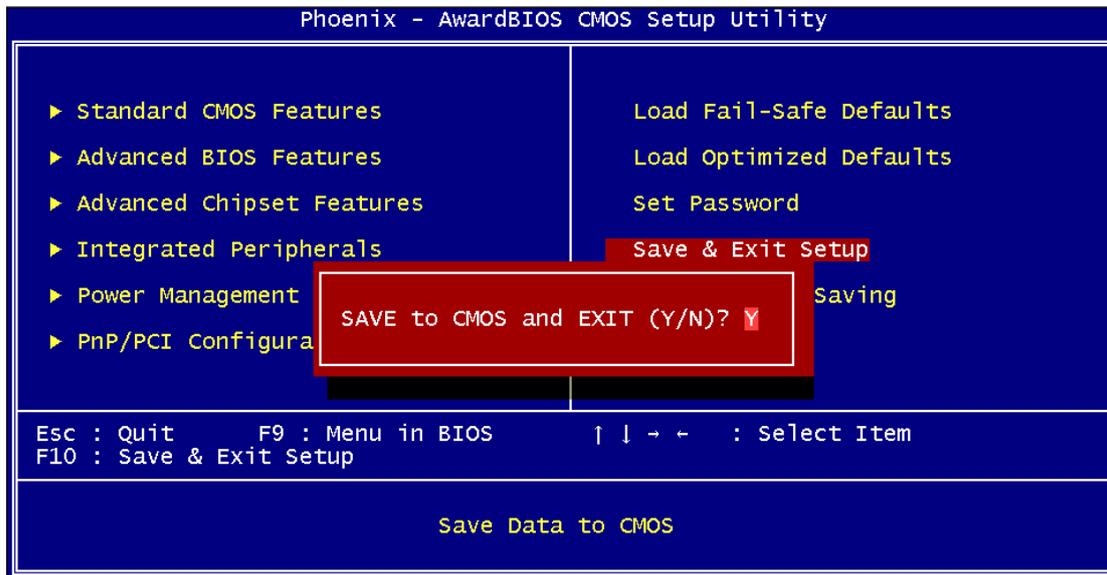
PASSWORD DISABLED.

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration. Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer. You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to "System", the password will be required both at boot and at entry to Setup. If set to "Setup", prompting only occurs when trying to enter Setup

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4.5.11 Exit Selecting

4.5.11.1 Save & Exit Setup

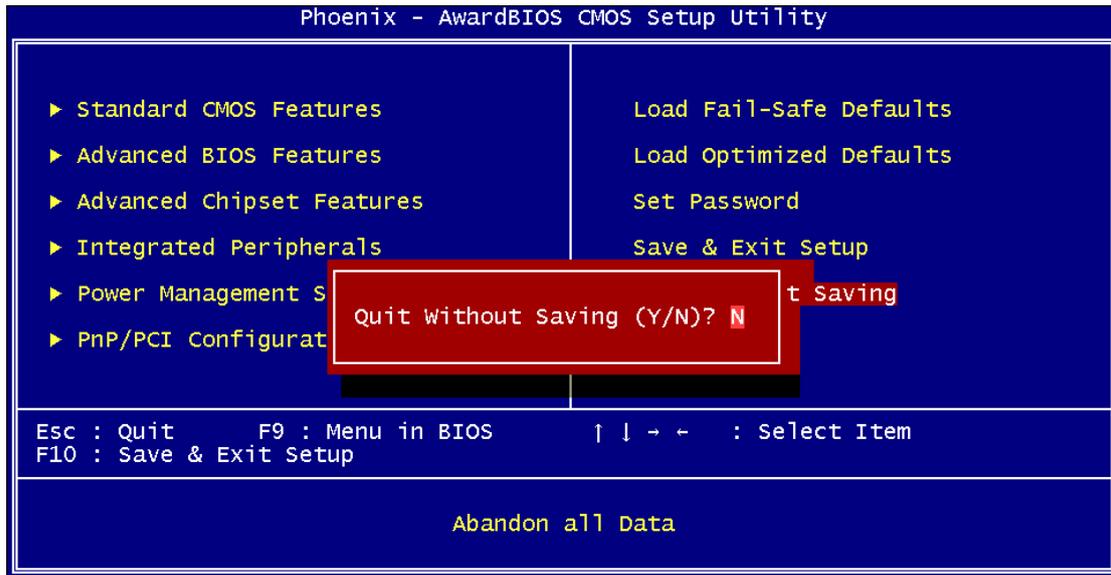


Pressing <Enter> on this item asks for confirmation:



Pressing "Y" stores the selections made in the menus in CMOS – a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

4.5.11.2 Exit Without Saving



Pressing <Enter> on this item asks for confirmation:



This allows you to exit Setup without storing in CMOS any change. The previous selections remain in effect. This exits the Setup utility and restarts your computer

5. Driver Installation

5.1 Driver installation for Ethernet Adapter

5.1.1 Windows 9x

The best way to install the driver for the Ethernet controller is to use the plug and play system of Windows 9x. The following procedures illustrate how the installation can be done.

1. If a driver for the Ethernet controller is already installed this must be removed first. This can be done by the following steps shown below.
 - Click the 'Start' button, click on 'Settings' and on 'Control panel' to open the control panel.

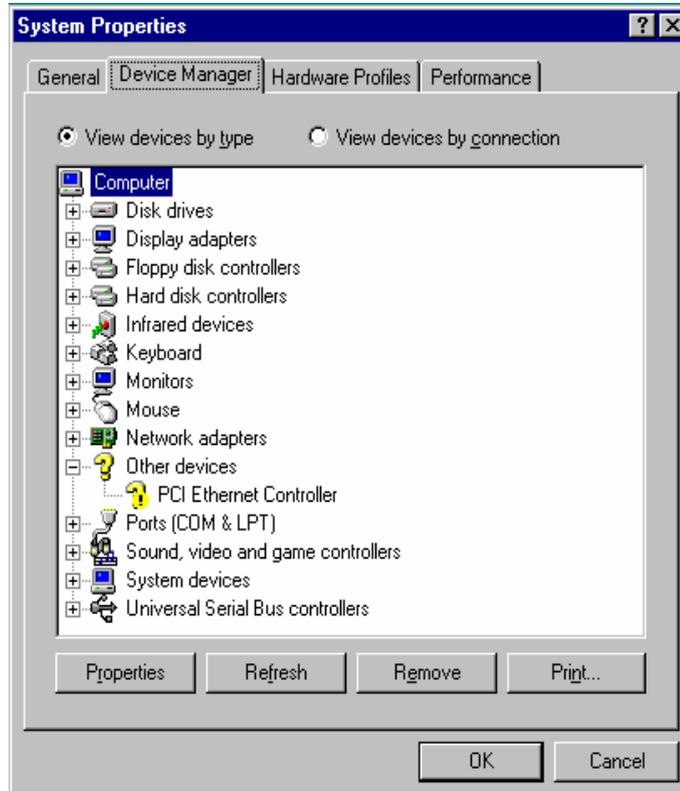
Your display should now look as below (possibly with different size and icons):



- Double click the 'System' icon (highlighted above).
- Select the 'Device Manager' tab.

- If the 'Network adapters' line is present, expand the line and remove the PCI Ethernet Controller adapters. This is done by selecting the line and clicking the 'Remove' button.

Before removal of the adapter(s), your screen might look like this:

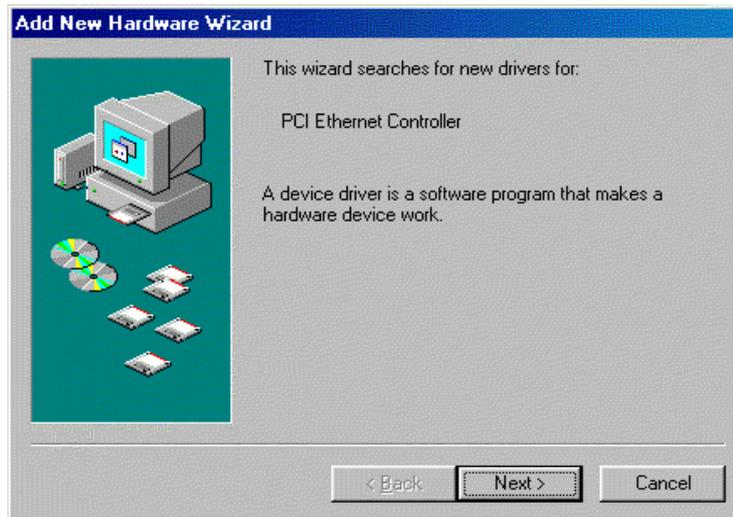


- When all adapters are removed (or none were present), a new driver can be installed.

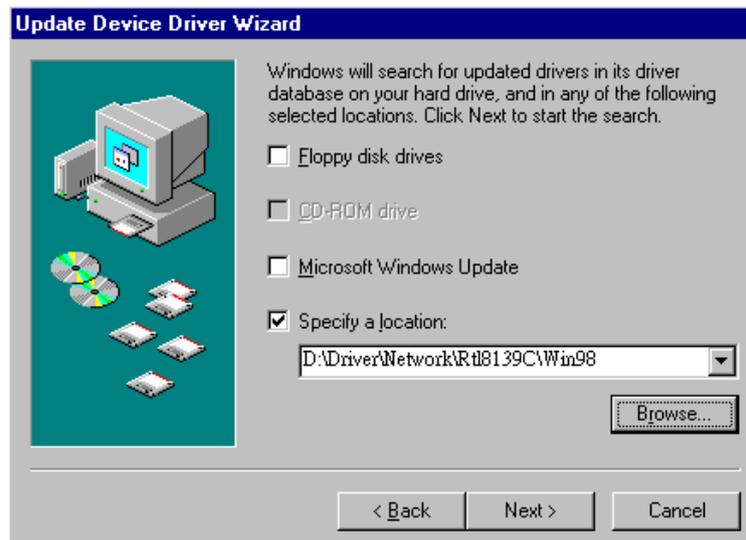
2. Reboot the computer.

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3. During the boot the network adapter should be detected as shown below:



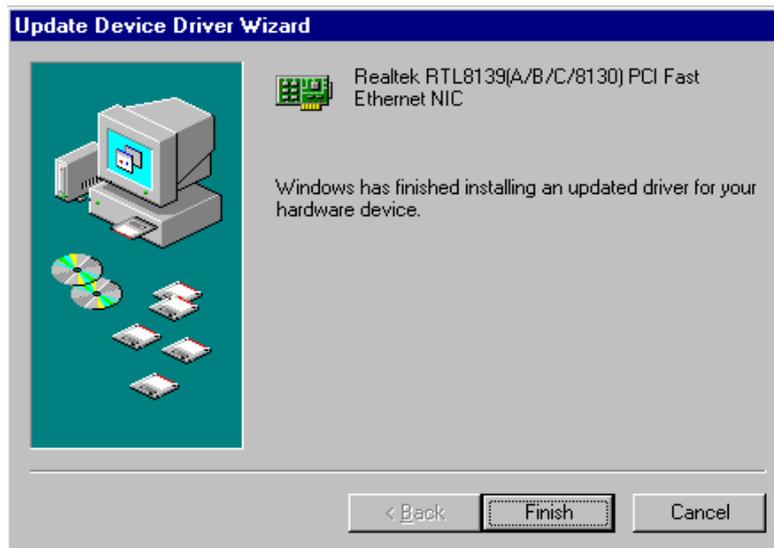
4. Specify the location of network adapter and click 'Next' (see below).



5. Click the 'Next' button.



6. Click the 'Finish' button.



7. Depending on the configuration, a request for the windows disks or CD-ROM may be necessary. Insert the disk / CD-ROM and click the 'OK' button. An entry of the directory for the files may then be required. After typing the path name, click the 'OK' button.

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- To complete the installation, reboot the computer by clicking the 'Yes' button in the window shown below.



- After the system restarts, the network adapter should be installed. Protocols, clients etc. may now be installed for the network in use.
- Further configuration of the adapter may be made in the 'Advanced' section of the driver properties. These options may be accessed through the 'Network' icon in the control panel (Select the network adapter, click the 'Properties' button and select the 'Advanced' tab).

5.2 Driver Installation for Display Adapter

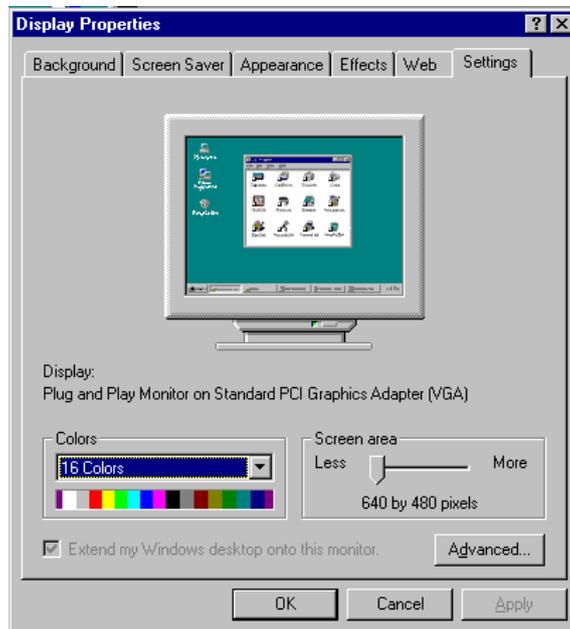
5.2.1 Windows 9x

The following steps will install the display driver for the 'Silicon Motion LynxEM+' display controller.

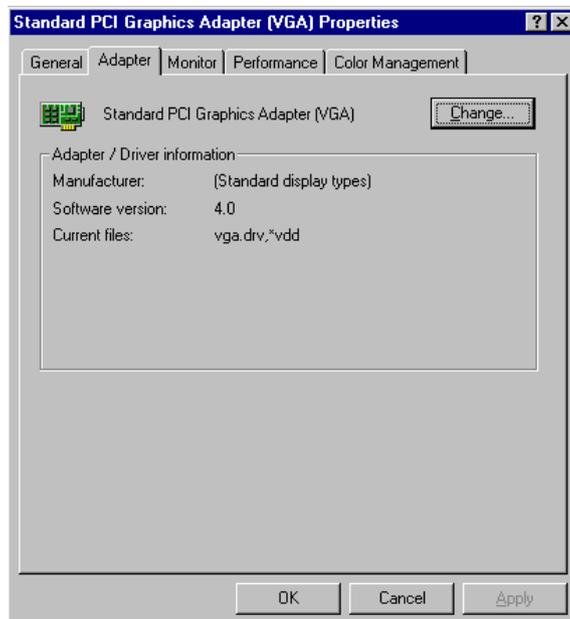
- Click the 'Start' button on the task bar, select 'Settings' and 'Control Panel' from the sub-menu. This should start the Control Panel as shown below:



2. Double click the 'Display' icon and select the 'Settings' tab as shown below.



3. Click the 'Advanced...' button. This will show the following window. Click the 'Change...' button in the Adapter Type frame to select another driver. Your display will probably have another driver than the 'Standard PCI Graphics Adapter (VGA)' installed at this moment.



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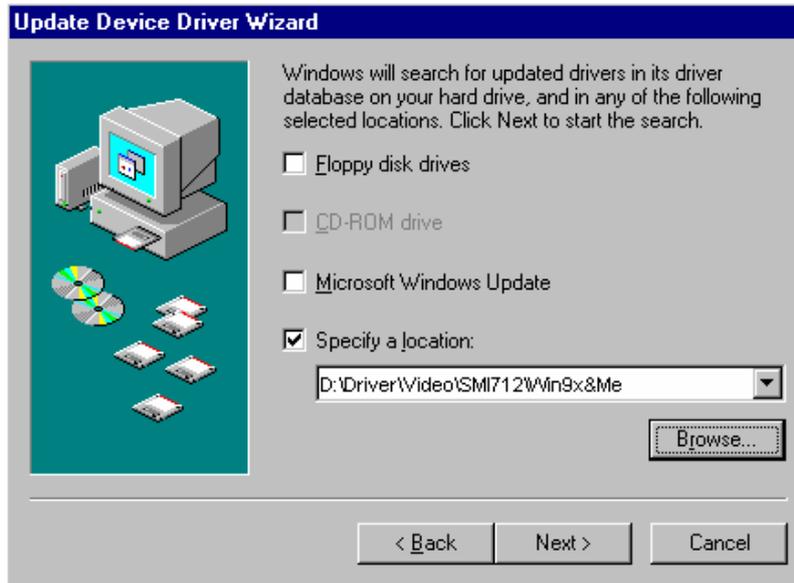
4. Click the 'Next' to update the display driver.



5. Click the 'Next' to continue the display driver installation.



6. Locate the path of Graphics adapter driver and click the 'Next' button.



7. The driver files will now be read and the display adapter is shown as the following. Click the 'Next' button to install the display driver.



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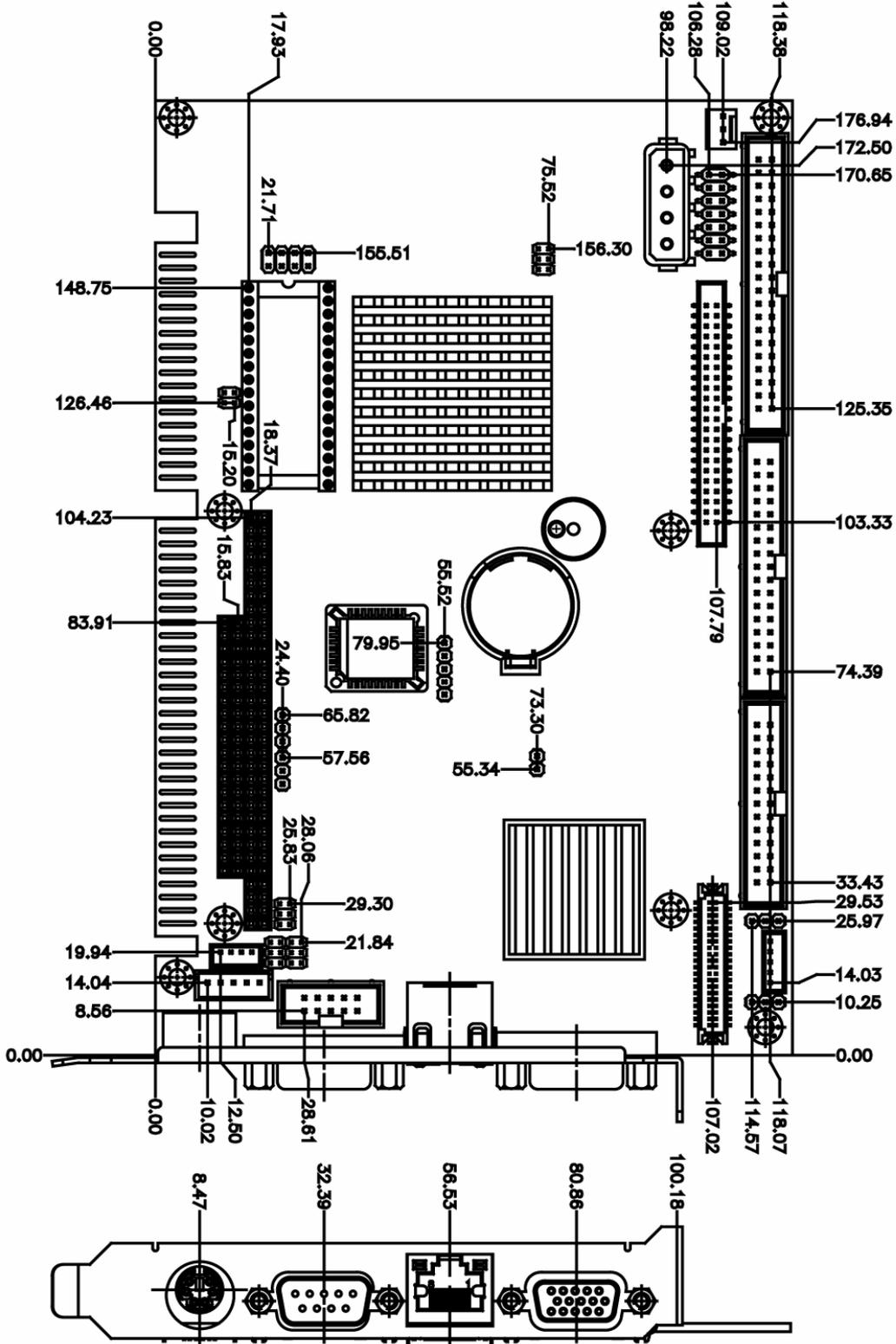
8. Click the *'Finish'* button.

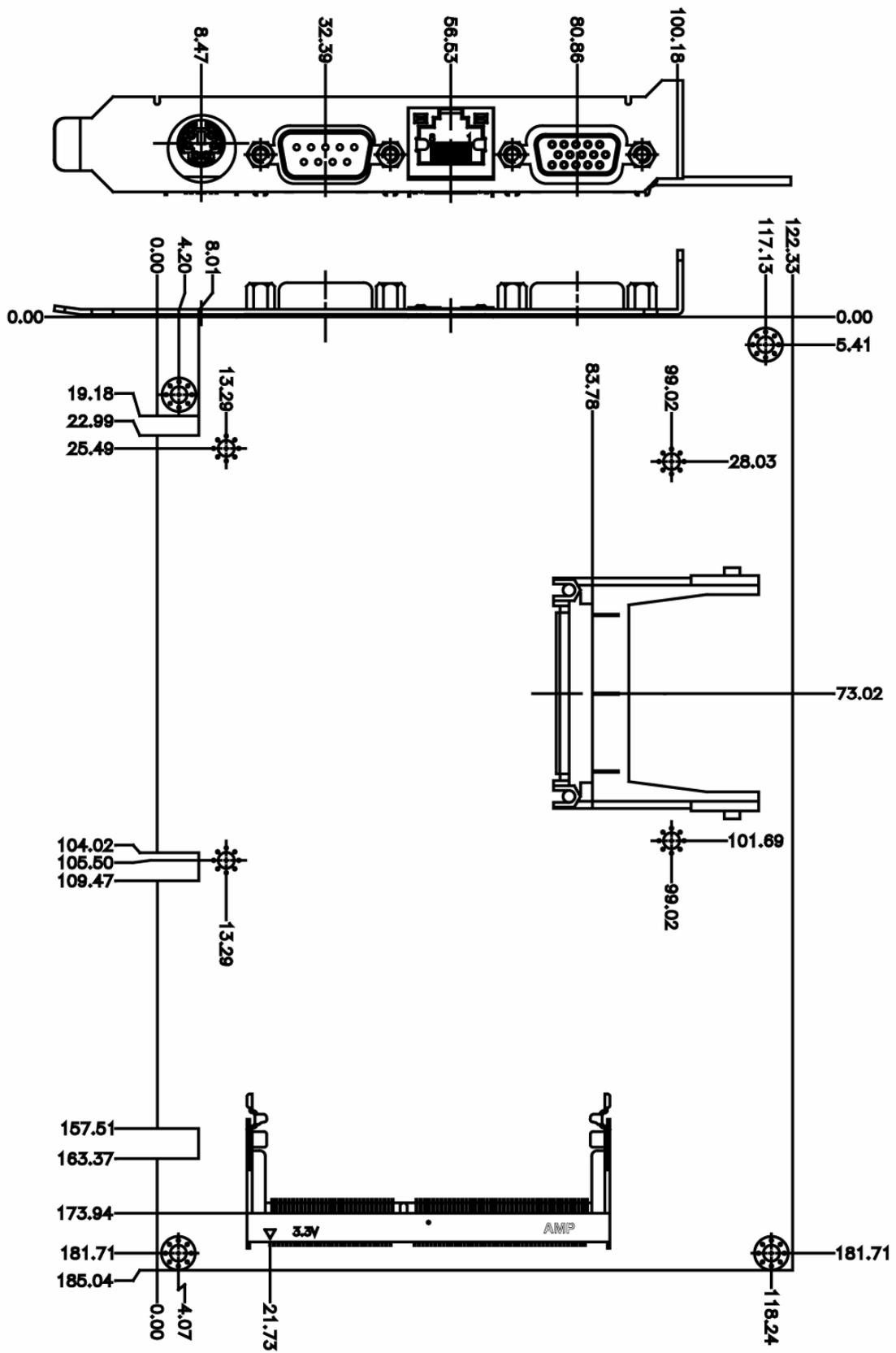


9. To complete the display driver installation, reboot the computer by clicking the *'Yes'* button in the window shown below.



6. Measurement Drawing





Appendix A: BIOS Revisions

BIOS Rev.

New Features

Bugs/Problems Solved

Known Problems

Appendix B: System Resources

Memory Map

The following table indicates memory map of ECB-641. The address ranges specify the runtime code length.

Address Range	Description	Note
00000000h-0009FFFFh	System board extension for PnP BIOS	
000A0000h-000AFFFFh	Silicon Motion LynxEM+	
000B0000h-000BFFFFh	Silicon Motion LynxEM+	
000C0000h-000CBFFFFh	Silicon Motion LynxEM+	
000F0000h-000F3FFFh	Motherboard resources	
000F4000h-000F7FFFh	Motherboard resources	
000F8000h-000FBFFFh	Motherboard resources	
000FC000h-000FFFFFh	Motherboard resources	
00100000h-00FFFFFFh	System board extension for PnP BIOS	
0D000000h-0DFFFFFFh	Silicon Motion LynxEM+	
0E000000h-0E0000FFh	RealtekRTL8139 (A/B/C/8130) PCI Fast Ethernet NIC	
10000000h-EFFFFFFFh	Motherboard resources	
FEE00000h-FEE0FFFFh	System board extension for PnP BIOS	
FFFE0000h-FFFFFFFh	System board extension for PnP BIOS	

I/O – Map

The board incorporates a fully ISA Bus Compatible interface. The drive capabilities allow for up to four external PC/104 modules to be driven without external data buffers. The accessible I/O area on the ISA-bus is 64Kbytes with 16 address bits, whereas the accessible memory area is 16Mbytes with 24 address bits.

Certain I/O addresses are subject to change during boot as PnP managers may relocate devices or functions. The addresses shown in the table are typical locations.

I/O Port	Description	Note
0000h-000Fh	Direct memory access controller	
0020h-0021h	Programmable interrupt controller	
0040h-0043h	System timer	
0060h-0060h	Standard 101/102 – key or Microsoft Natural Keyboard	
0061h-0061h	System speaker	
0064h-0064h	Standard 101/102 – key or Microsoft Natural Keyboard	
0070h-0071h	System CMOS/real time clock	
0081h-0083h	Direct memory access controller	
0087h-0087h	Direct memory access controller	
0089h-008Bh	Direct memory access controller	
008Fh-0091h	Direct memory access controller	
00A0h-00A1h	Programmable interrupt controller	
00C0h-00DFh	Direct memory access controller	
00F0h-00FFh	Numeric data processor	
0170h-0177h	Secondary IDE controller (single fifo)	1
0170h-0177h	Standard Dual PCI IDE Controller	1
01F0h-01F7h	Standard Dual PCI IDE Controller	1
01F0h-01F7h	Primary IDE controller (single fifo)	1

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I/O Port	Description	Note
02F8h-02FFh	Communications Port (COM2)	1
0376h-0376h	Secondary IDE controller (single fifo)	1
0376h-0376h	Standard Dual PCI IDE Controller	1
0378h-037Fh	Printer port (LPT1)	1
03B0h-03BBh	Silicon Motion LynxEM+	
03C0h-03DFh	Silicon Motion LynxEM+	
03F2h-03F5h	Standard Floppy Disk Controller	1
03F6h-03F6h	Standard Dual PCI IDE Controller	1
03F6h-03F6h	Primary IDE controller (single fifo)	1
03F8h-03FFh	Communications Port (COM1)	1
04D0h-04D1h	PCI bus	1
0CF8h-0CFFh	PCI bus	
E000h-E00Fh	Standard Dual PCI IDE Controller	1
E000h-E007h	Primary IDE controller (single fifo)	1
E008h-E00Fh	Secondary IDE controller (single fifo)	1
E400h-E4FFh	Realtek RTL8139 / 810X Family PCI Fast Ethernet NIC	

Note:

1. The usage of these I/O addresses depends on the choices made in the Evalue setup screen. The I/O addresses are fully usable for PC/104 interface if the corresponding on-board unit is disabled in the setup screen.

Interrupt Usage

Interrupt	Description	Note
IRQ0	System timer	
IRQ1	Standard 101/102-Key or Microsoft Natural Keyboard	
IRQ2	Programmable interrupt controller	
IRQ3	Communications Port (COM2)	
IRQ4	Communications Port (COM1)	
IRQ6	Standard Floppy Disk Controller	
IRQ7	Printer Port (LPT1)	
IRQ8	System CMOS/real time clock	
IRQ10	Sillicon Motion LynxEM+	
IRQ10	IRQ Holder for PCI Steering	
IRQ11	IRQ Holder for PCI Steering	
IRQ11	Realtek RTL8139 / 810X Family PCI Fast Ethernet NIC	
IRQ12	PS/2 Compatible Mouse Port	
IRQ13	Numeric data processor	
IRQ14	Primary IDE controller (single fifo)	
IRQ14	Standard Dual PCI IDE Controller	
IRQ15	Standard Dual PCI IDE Controller	
IRQ15	Secondary IDE controller (single fifo)	

DMA-channel Usage

DMA-channel	Description	Note
DMA2	Standard Floppy Disk Controller	
DMA4	Direct memory access controller	

Appendix C: AWARD BIOS Error Message

During the power-on self test (POST), the BIOS either sounds a beep code or displays a message when it detects a correctable error.

Following is a list of POST messages for the ISA BIOS kernel. Specific chipset ports and BIOS extensions may include additional messages. An error message may be followed by a prompt to press F1 to continue or press DEL to enter Setup.

Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

CMOS BATTERY HAS FAILED

CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

DISPLAY SWITCH IS SET INCORRECTLY

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

EISA Configuration Checksum Error PLEASE RUN EISA CONFIGURATION UTILITY

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the card is installed firmly in the slot.

EISA Configuration Is Not Complete PLEASE RUN EISA CONFIGURATION UTILITY

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note: When either of these errors appear, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

ERROR INITIALIZING HARD DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

Invalid EISA Configuration PLEASE RUN EISA CONFIGURATION UTILITY

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

MEMORY SIZE HAS CHANGED SINCE LAST BOOT

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

OFFENDING ADDRESS NOT FOUND

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

OFFENDING SEGMENT:

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

PRESS A KEY TO REBOOT

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

Should Be Empty But EISA Board Found PLEASE RUN EISA CONFIGURATION UTILITY

A valid board ID was found in a slot that was configured as having no board ID.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Should Have EISA Board But Not Found PLEASE RUN EISA CONFIGURATION UTILITY

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Slot Not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Wrong Board In Slot PLEASE RUN EISA CONFIGURATION UTILITY

The board ID does not match the ID stored in the EISA non-volatile memory.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

User's Manual

FLOPPY DISK(S) fail (80) → Unable to reset floppy subsystem.

FLOPPY DISK(S) fail (40) → Floppy Type mismatch.

Hard Disk(s) fail (80) → HDD reset failed

Hard Disk(s) fail (40) → HDD controller diagnostics failed.

Hard Disk(s) fail (20) → HDD initialization error

Hard Disk(s) fail (10) → Unable to recalibrate fixed disk.

Hard Disk(s) fail (08) → Sector Verify failed.

Keyboard is locked out - Unlock the key.

BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

Keyboard error or no keyboard present

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

Manufacturing POST loop.

System will repeat POST procedure infinitely while the P15 of keyboard controller is pull low. This is also used for M/B burn in test.

BIOS ROM checksum error - System halted.

The checksum of ROM address F0000H-FFFFFFH is bad.

Memory test fail.

BIOS reports the memory test fail if the onboard memory is tested error.

Appendix D: AWARD BIOS POST Codes

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.

POST (hex)	Description
15h	Reserved
16h	Initial Early_Init_Onboard_Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyril or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	<ol style="list-style-type: none"> 1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: <ul style="list-style-type: none"> -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0.
24h	Reserved
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer
28h	Reserved
29h	<ol style="list-style-type: none"> 1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed. 5. Invoke video BIOS.

POST (hex)	Description
2Ah	Reserved
2Bh	Reserved
2Ch	Reserved
2Dh	1. Initialize multi-language 2. Put information on screen display, including Award title, CPU type, CPU speed
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	Reserved
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program writes allocation for AMD K5 CPU.

POST (hex)	Description
4Fh	Reserved
50h	Initialize USB
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onboard_AUDIO switch.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache

POST (hex)	Description
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved
73h	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive. -ALT+F2 is pressed
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM.....
76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported. -If errors occur, report errors & wait for keys -If no errors occur or F1 key is pressed to continue: ♦Clear EPA or customization logo.
80h	Reserved

POST (hex)	Description
81h	Reserved
82h	<ol style="list-style-type: none"> 1. Call chipset power management hook. 2. Recover the text font used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	<ol style="list-style-type: none"> 1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	<ol style="list-style-type: none"> 1. Enable L2 cache 2. Program boot up speed 3. Chipset final initialization. 4. Power management final initialization 5. Clear screen & display summary table 6. Program K6 write allocation 7. Program P6 class write combining
95h	<ol style="list-style-type: none"> 1. Program daylight saving 2. Update keyboard LED & typematic rate
96h	<ol style="list-style-type: none"> 1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)